Litigation Search Report CRU 3999

Reexam Control No. 90/005,471

TO: Mark Reinhart **Location: CRU** **Art Unit : 3992** **Date: 04/15/06** **Case Serial Number: 90/005,471**	**From: James R. Matthews** **Location: CRU 3999** **RND 1C79** **Phone: (571) 272-4233** **JamesR.Matthews@uspto.gov**

Search Notes

U.S. Patent No- 5,598,525

1) I performed a KeyCite Search in Westlaw, which retrieves all history on the patent including any litigation.

2) I performed a search on the patent in Lexis CourtLink for any open dockets or closed cases.

3) I performed a search in Lexis in the Federal Courts and Administrative Materials databases for any cases found.

4) I performed a search in Lexis in the IP Journal and Periodicals database for any articles on the patent.

5) I performed a search in Lexis in the news databases for any articles about the patent or any articles about litigation on this patent.

Litigation was found

Westlaw.

Date of Printing: APR 13,2006

KEYCITE

CUS PAT 5598525 APPARATUS, SYSTEMS AND METHODS FOR CONTROLLING GRAPHICS AND VIDEO DATA IN MULTIMEDIA DATA PROCESSING AND DISPLAY SYSTEMS, Assignee: Cirrus Logic, Inc. (Jan 28, 1997)

History

=> 1 **APPARATUS, SYSTEMS AND METHODS FOR CONTROLLING GRAPHICS AND VIDEO DATA IN MULTIMEDIA DATA PROCESSING AND DISPLAY SYSTEMS,** US PAT 5598525, 1997 WL 1406522 (U.S. PTO Utility Jan 28, 1997) (NO. 376919)

Assignments

2 Assignee(s): BANK OF AMERICA NATIONAL TRUST & SAVINGS ASSOCIATION AS AGENT 1455 MARKET STREET SAN FRANCISCO, CALIFORNIA 94103, DATE RECORDED: Aug 29, 1996

3 Assignee(s): CIRRUS LOGIC, INC. 3100 WEST WARREN AVENUE FREMONT, CALIFORNIA 94538, DATE RECORDED: Jan 23, 1995

Patent Status Files

. Request for Re-Examination, (OG date: Nov 09, 1999)

. Certificate of Correction, (OG date: May 11, 1999)

. Certificate of Correction, (OG date: Dec 02, 1997)

Litigation Alert

7 LitAlert P1998-30-06, (Jul 08, 1998) Action Taken: A complaint was filed.

Prior Art

C 8 US PAT 5274753 APPARATUS FOR DISTINGUISHING INFORMATION STORED IN A FRAME BUFFER, Assignee: Apple Computer, Inc., (U.S. PTO Utility 1993)

C 9 US PAT 5257348 APPARATUS FOR STORING DATA BOTH VIDEO AND GRAPHICS SIGNALS IN A SINGLE FRAME BUFFER, Assignee: Apple Computer, Inc., (U.S. PTO Utility 1993)

C 10 US PAT 5341442 METHOD AND APPARATUS FOR COMPRESSION DATA BY GENERATING BASE IMAGE DATA FROM LUMINANCE AND CHROMINANCE COMPONENTS AND DETAIL IMAGE DATA FROM LUMINANCE COMPONENT, Assignee: SuperMac Technology, Inc., (U.S. PTO Utility 1994)

C 11 US PAT 5218432 METHOD AND APPARATUS FOR MERGING VIDEO DATA SIGNALS FROM MULTIPLE SOURCES AND MULTIMEDIA SYSTEM INCORPORATING SAME, Assignee: Tandy Corporation, (U.S. PTO Utility 1993)

C 12 US PAT 5229852 REAL TIME VIDEO CONVERTER PROVIDING SPECIAL EFFECTS, Assignee: RasterOps Corporation, (U.S. PTO Utility 1993)

C 13 US PAT 5365278 SIDE BY SIDE TELEVISION PICTURES, Assignee: Thomson Consumer Electronics, (U.S. PTO Utility 1994)

C 14 US PAT 5406306 SYSTEM FOR, AND METHOD OF DISPLAYING INFORMATION FROM A GRAPHICS MEMORY AND A VIDEO MEMORY ON A DISPLAY MONITOR, Assignee: Brooktree Corporation, (U.S. PTO Utility 1995)

C 15 US PAT 5341318 SYSTEM FOR COMPRESSION AND DECOMPRESSION OF VIDEO DATA USING DISCRETE COSINE TRANSFORM AND CODING TECHNIQUES, Assignee: C-Cube Microsystems, Inc., (U.S. PTO Utility 1994)

C 16 US PAT 4991122 WEIGHTED MAPPING OF COLOR VALUE INFORMATION ONTO A DISPLAY SCREEN, Assignee: General Parametrics Corporation, (U.S. PTO Utility 1991)

Docket

US District Court Civil Docket

U.S. District - California Northern
(San Francisco)

3:98cv2700

Cirrus Logic, Inc v. Ati Technologies Inc

This case was retrieved from the court on Tuesday, May 24, 2005

Date Filed:	**07/08/1998**	Class Code:	**TERMED PROTO AO279 STAY ENET**
Assigned To:	**Judge Susan Illston**	Closed:	**yes**
Referred To:		Statute:	**15:1126**
Nature of suit:	**Patent (830)**	Jury Demand:	**Both**
Cause:	**Patent Infringement**	Demand Amount:	**$0**
Lead Docket:	**None**	NOS Description:	**Patent**
Other Docket:	**None**		
Jurisdiction:	**Federal Question**		

Litigants	Attorneys
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Documents

Retrieve Document(s)

	Availability	Date	No.	Proceeding Text (Filter)
	Runner	07/08/1998	1	COMPLAINT Summons(es) issued; Fee status pd entered on 7/8/98 in the amount No. 48454); jury demand [3:98-cv-02700] (ga) [Entry date 07/09/98]
	Runner	07/08/1998	2	ORDER RE COURT PROCEDURE and SCHEDULE by Judge Susan Illston : Proof of s 8/24/98 ; counsels' case management statement to be filed by 10/27/98 ; initial c conference will be held 2:00 11/6/98 . (cc: all counsel) (ga) [Entry date 07/09/98
	Runner	07/08/1998	--	Docket Modification (Administrative) to for referral to Early Neutral Evaluation (AD 02700] (ga) [Entry date 07/09/98]
	Runner	07/09/1998	--	REPORT on the filing of an action regarding Trademark (cc: form mailed to registe (ga)
	Runner	08/24/1998	3	RETURN OF SERVICE executed upon defendant ATI Technologies Inc on 8/6/98 [3 [Entry date 08/25/98]
	Runner	08/31/1998	4	ANSWER to complaint [1-1] and COUNTERCLAIM; jury demand by defendant ATI T against Plaintiff Cirrus Logic, Inc. [3:98-cv-02700] (ga) [Entry date 09/02/98]
	Runner	09/21/1998	5	ANSWER TO COUNTERCLAIM [4-2] by Counter-defendant Cirrus Logic, Inc. [3:98- date 09/24/98]
	Runner	10/08/1998	6	CLERK'S NOTICE of appointment of evaluator, Lynn H. Pasahow [3:98-cv-02700] (
	Runner	10/14/1998	7	LETTER dated 10/13/98 from Michael A. Jacobs from Cirrus Logic, Inc. re initial dis 02700] (ga) [Entry date 10/19/98]
	Runner	10/23/1998	8	EVALUATOR'S Letter to Counsel ENE phone conference set for 10:00 10/26/98 [3:
	Runner	10/27/1998	10	CERTIFICATION of discussion of ADR options by defendant ATI Technologies Inc . [Entry date 10/28/98]
	Runner	10/27/1998	11	CERTIFICATION of discussion of ADR options by Plaintiff Cirrus Logic, Inc. . [3:98- date 10/28/98]
	Runner	10/27/1998	12	CASE MANAGEMENT STATEMENT and PROPOSED ORDER filed. [3:98-cv-02700] (g 10/28/98]
	Runner	10/28/1998	9	EVALUATOR'S Letter to Counsel ENE hearing will be held 9:30 12/7/98 ; [3:98-cv-
	Runner	11/10/1998	13	MINUTES: (C/R none; hearing of 11/6/98) INITIAL CASE MANAGEMENT CONFERE Hearing set for 9:00 5/14/99 ; Discovery cutoff 7/15/99 ; deadline for discovery fr 7/15/99 ; All motions will be filed by 6/11/99 ; All motions hearing date 9:00 7/16 conference will be held 3:30 8/17/99 ; Jury Trial set for 8:30 8/30/99 ; parties wil to occur on 3/2/99 and 3/3/99 at 3:30pm; [3:98-cv-02700] (ga) [Entry date 11/1
	Runner	11/12/1998	14	SCHEDULING ORDER by Judge Susan Illston : ; tutorial conference for 3:30 3/2/9 6/11/99 ; all motions hearing on 9:00 7/16/99 ; pretrial conference set for 8:30 8, for 8:30 8/30/99 (cc: all counsel) [3:98-cv-02700] (ga) [Entry date 11/18/98]
	Runner	12/15/1998	15	CERTIFICATION OF ADR SESSION ENE session held on 9:30 12/7/98 ; ENE proces neutral Early Neutral Evaluator Lynn H. Pasahow. Follow up phone conference exp (kq)
	Runner	01/04/1999	16	EVALUATOR'S Letter to Counsel confirming that another telephone conference is s Thursday, January 14, 1999 to continue reporting the parties' progress in continui discussion. [3:98-cv-02700] (kq)
	Runner	02/24/1999	17	REQUEST by defendant ATI Technologies Inc to Allow Entry of Equipment [3:98-cv date 03/01/99]
	Runner	02/25/1999	18	ORDER by Judge Susan Illston granting request [17-1] (Date Entered: 3/1/99) (c cv-02700] (ga) [Entry date 03/01/99]

☐	Runner	03/01/1999	20	ORDER by Judge Susan Illston granting request [17-1] (Date Entered: 3/4/99) (c cv-02700] (ga) [Entry date 03/04/99]
☐	Runner	03/03/1999	19	EVALUATOR'S Letter to Counsel whether the parties would like to continue with EN (kq)
☐	Runner	03/15/1999	23	AMENDED ANSWER [4-1] by defendant ATI Technologies Inc; jury demand [3:98- [Entry date 03/16/99]
☐	Runner	03/15/1999	--	AMENDED COUNTERCLAIM [4-2] by Counter-claimant ATI Technologies Inc [3:98- [Entry date 03/16/99]
☐	Runner	03/15/1999	24	APPLICATION by defendant ATI Technologies Inc for Ruffin B. Cordell, Linda Liu Kc McKeon and Brian R. Nester to appear as counsel pro hac vice. [3:98-cv-02700] (03/16/99]
☐	Runner	03/15/1999	25	DECLARATION by Ruffin B. Cordell on behalf of defendant ATI Technologies Inc re [3:98-cv-02700] (cgd) [Entry date 03/16/99]
☐	Runner	03/15/1999	26	DECLARATION by Michael J. McKeon on behalf of defendant ATI Technologies Inc [3:98-cv-02700] (cgd) [Entry date 03/16/99]
☐	Runner	03/15/1999	27	DECLARATION by Linda Liu Kordziel on behalf of defendant ATI Technologies Inc r [3:98-cv-02700] (cgd) [Entry date 03/16/99]
☐	Runner	03/15/1999	28	DECLARATION by Brian R. Nester on behalf of defendant ATI Technologies Inc re a [3:98-cv-02700] (cgd) [Entry date 03/16/99]
☐	Runner	03/15/1999	29	PROOF OF SERVICE by ATI Technologies Inc of answer [23-1], amend/amended c application [24-1], declaration [25-1], declaration [26-1], declaration [27-1], decl cv-02700] (cgd) [Entry date 03/16/99]
☐	Runner	03/16/1999	21	EVALUATOR'S Letter to Counsel that Early Neutral Evaluation should be deemed c 02700] (kq)
☐	Runner	03/16/1999	22	ADR CLERK'S NOTICE of Removal from Early Neutral Evaluation.ENE PROCESS CO 02700] (kq)
☐	Runner	03/17/1999	30	EXPEDITED MOTION before Judge Susan Illston by Plaintiff Cirrus Logic, Inc. for le Chart [3:98-cv-02700] (cgd) [Entry date 03/18/99]
☐	Runner	03/17/1999	31	DECLARATION by Grant L. Kim on behalf of Plaintiff Cirrus Logic, Inc. re motion fo Claim Chart [30-1]UNDER SEAL. [3:98-cv-02700] (cgd) [Entry date 03/18/99]
☐	Runner	03/17/1999	32	PROOF OF SERVICE by Cirrus Logic, Inc. of motion for leave to amend Claim Chart [31-1] [3:98-cv-02700] (cgd) [Entry date 03/18/99]
☐	Runner	03/17/1999	33	ORDER by Judge Susan Illston granting application [24-1] for attorney to appear p Entered: 3.23.99) (cc: all counsel) [3:98-cv-02700] (cgd) [Entry date 03/23/99]
☐	Runner	03/17/1999	35	STIPULATION and ORDER regarding ATI's first amended answer by Judge Susan Il counsel) [3:98-cv-02700] (cgd) [Entry date 03/23/99]
☐	Runner	03/18/1999	34	STIPULATION and ORDER by Judge Susan Illston : setting hearing on motion for le Chart [30-1] 3:30 3/31/99 (cc: all counsel) [3:98-cv-02700] (cgd) [Entry date 03/
☐	Runner	03/23/1999	36	NOTICE by Cirrus Logic, Inc. [34-1] order [3:98-cv-02700] (cgd) [Entry date 03/2
☐	Runner	03/24/1999	37	OPPOSITION by defendant ATI Technologies Inc to motion for leave to amend Clai [3:98-cv-02700] (cgd) [Entry date 03/25/99]
☐	Runner	03/24/1999	38	DECLARATION by John W. Thornburgh on behalf of defendant ATI Technologies In UNDER SEAL. [3:98-cv-02700] (cgd) [Entry date 03/25/99]
☐	Runner	03/24/1999	39	PROOF OF SERVICE by ATI Technologies Inc of opposition [37-1], declaration [38- (cgd) [Entry date 03/25/99]
☐	Runner	03/26/1999	40	REPLY by Plaintiff Cirrus Logic, Inc. in support of its expedited motion for leave to [30-1] [3:98-cv-02700] (cgd) [Entry date 03/29/99]
☐	Runner	03/31/1999	41	APPLICATION of Seth E. Brown to appear pro hac vice for Plaintiff Cirrus Logic, Inc POINTS AND AUTHORITIES in support thereof. [3:98-cv-02700] (cgd) [Entry date
☐	Runner	03/31/1999	42	DECLARATION by Seth E. Brown on behalf of Plaintiff Cirrus Logic, Inc. re applicati 02700] (cgd) [Entry date 04/01/99]
☐	Runner	04/01/1999	43	ORDER by Judge Susan Illston granting application [41-1] for attorney Seth E. Bro vice (Date Entered: 4.5.99) (cc: all counsel) [3:98-cv-02700] (cgd) [Entry date 0
☐	Runner	04/02/1999	44	SUPPLEMENTAL CLAIM CONSTRUCTION STATEMENT by Plaintiff Cirrus Logic, Inc. [(cgd) [Entry date 04/05/99]
☐	Runner	04/02/1999	45	ORDER by Judge Susan Illston GRANTING Plaintiff's motion for leave to amend Cla AMENDED PRETRIAL AND TRIAL DATES: Discovery cutoff set for 10/1/99 ; Deadlir filings is 9/3/99 ; All motions will be heard by 9:00 10/8/99 ; Pretrial conference s 11/16/99 ; Jury trial will be held 8:30 11/29/99 ; (Date Entered: 4.5.99) (cc: all 02700] (cgd) [Entry date 04/05/99]
☐	Runner	04/02/1999	47	FIRST AMENDED CLAIM CHART by Plaintiff Cirrus Logic, Inc. pursuant to Local Rul [3:98-cv-02700] (cgd) [Entry date 04/07/99]
☐	Runner	04/05/1999	46	REPORTER'S TRANSCRIPT; Date of proceedings: March 2, 1999 (C/R: Leo Mankie 02700] (cgd) [Entry date 04/06/99]
☐	Runner	04/06/1999	48	NOTICE by Cirrus Logic, Inc. [43-2] order [3:98-cv-02700] (cgd) [Entry date 04/0

☐				
☐	Runner	04/09/1999	49	MOTION with MEMORANDUM OF POINTS AND AUTHORITIES IN SUPPORT before J Plaintiff Cirrus Logic, Inc. for leave to file First Amended Complaint [3:98-cv-0270 04/13/99]
☐	Runner	04/09/1999	50	DECLARATION by Mani Adeli on behalf of Plaintiff Cirrus Logic, Inc. re motion for l Amended Complaint [49-1] [3:98-cv-02700] (cgd) [Entry date 04/13/99]
☐	Runner	04/12/1999	51	STIPULATION and ORDER by Judge Susan Illston : extending time for Cirrus Logic, ATI's amended answer and counterclaim until 4/12/99. (cc: all counsel) [3:98-cv- date 04/13/99]
☐	Runner	04/13/1999	52	EXPEDITED MOTION before Judge Susan Illston by Plaintiff Cirrus Logic, Inc. for pr confidential information UNDER SEAL. [3:98-cv-02700] (cgd) [Entry date 04/15/9
☐	Runner	04/13/1999	53	DECLARATION by Russell B. Hill on behalf of Plaintiff Cirrus Logic, Inc. re motion f confidential information [52-1] UNDER SEAL. [3:98-cv-02700] (cgd) [Entry date 0
☐	Runner	04/13/1999	54	DECLARATION by Steven A. Shaw on behalf of Plaintiff Cirrus Logic, Inc. re motion of confidential information [52-1] [3:98-cv-02700] (cgd) [Entry date 04/15/99]
☐	Runner	04/13/1999	55	DECLARATION by Robert F. Donohue on behalf of Plaintiff Cirrus Logic, Inc. re mot order of confidential information [52-1] [3:98-cv-02700] (cgd) [Entry date 04/15/
☐	Runner	04/13/1999	--	RECEIVED Proposed Order (Cirrus Logic, Inc.) re: motion for protective order of information [52-1] [3:98-cv-02700] (cgd) [Entry date 04/15/99]
☐	Runner	04/13/1999	56	PROOF OF SERVICE by Cirrus Logic, Inc. of motion for protective order of confiden 1], declaration [53-1], declaration [54-1], declaration [55-1], order received [0-0] (cgd) [Entry date 04/15/99]
☐	Runner	04/13/1999	57	MOTION before Judge Susan Illston by defendant ATI Technologies Inc for protecti depositions. [3:98-cv-02700] (cgd) [Entry date 04/15/99]
☐	Runner	04/13/1999	58	DECLARATION by John W. Thornburgh on behalf of defendant ATI Technologies In protective order re depositions [57-1] UNDER SEAL. [3:98-cv-02700] (cgd) [Entry
☐	Runner	04/13/1999	59	PROOF OF SERVICE by ATI Technologies Inc of motion for protective order re depc declaration [58-1] [3:98-cv-02700] (cgd) [Entry date 04/15/99]
☐	Runner	04/15/1999	60	NOTICE by Cirrus Logic, Inc. [51-2] order [3:98-cv-02700] (cgd) [Entry date 04/1
☐	Runner	04/15/1999	61	STIPULATION and ORDER by Judge Susan Illston : granting motion for protective [57-1], granting motion for protective order of confidential information [52-1] (cc: cv-02700] (cgd) [Entry date 04/16/99]
☐	Runner	04/16/1999	62	OPPOSITION by defendant ATI Technologies Inc to Cirrus' motion for protective or information [52-1] UNDER SEAL. [3:98-cv-02700] (cgd) [Entry date 04/19/99]
☐	Runner	04/16/1999	63	DECLARATION by Sally J. Daub on behalf of defendant ATI Technologies Inc re opp UNDER SEAL. [3:98-cv-02700] (cgd) [Entry date 04/19/99]
☐	Runner	04/16/1999	64	DECLARATION by John W. Thornburgh on behalf of defendant ATI Technologies In UNDER SEAL. [3:98-cv-02700] (cgd) [Entry date 04/19/99]
☐	Runner	04/16/1999	65	PROOF OF SERVICE by ATI Technologies Inc of opposition [62-1], declaration [63- [3:98-cv-02700] (cgd) [Entry date 04/19/99]
☐	Runner	04/16/1999	66	OPPOSITION by Plaintiff Cirrus Logic, Inc. to ATI's motion for protective order re d UNDER SEAL. [3:98-cv-02700] (cgd) [Entry date 04/19/99]
☐	Runner	04/16/1999	67	DECLARATION by Russell B. Hill on behalf of Plaintiff Cirrus Logic, Inc. re oppositio SEAL. [3:98-cv-02700] (cgd) [Entry date 04/19/99]
☐	Runner	04/16/1999	68	EX-PARTE APPLICATION before Judge Susan Illston by Plaintiff Cirrus Logic, Inc. to motion for leave to file First Amended Complaint [49-1] [3:98-cv-02700] (cgd) [E
☐	Runner	04/16/1999	69	DECLARATION by Mani Adeli on behalf of Plaintiff Cirrus Logic, Inc. re motion to sh for leave to file First Amended Complaint [49-1] [68-1] [3:98-cv-02700] (cgd) [Er
☐	Runner	04/16/1999	--	RECEIVED Proposed Order (Cirrus Logic, Inc.) re: motion to shorten time on mot First Amended Complaint [49-1] [68-1] [3:98-cv-02700] (cgd) [Entry date 04/19/
☐	Runner	04/16/1999	70	PROOF OF SERVICE of motion to shorten time on motion for leave to file First Ame 1] [68-1], order received [0-0], declaration [69-1] [3:98-cv-02700] (cgd) [Entry
☐	Runner	04/19/1999	71	OPPOSITION by defendant ATI Technologies Inc to Plaintiff's motion to shorten tim to file First Amended Complaint [49-1] [68-1] [3:98-cv-02700] (cgd) [Entry date
☐	Runner	04/20/1999	72	REPLY MEMORANDUM by defendant ATI Technologies Inc in support of motion for depositions [57-1] UNDER SEAL. [3:98-cv-02700] (cgd) [Entry date 04/22/99]
☐	Runner	04/20/1999	73	DECLARATION by John W. Thornburgh on behalf of defendant ATI Technologies In [72-1] UNDER SEAL. [3:98-cv-02700] (cgd) [Entry date 04/22/99]
☐	Runner	04/20/1999	74	PROOF OF SERVICE by ATI Technologies Inc of memorandum [72-1], declaration [02700] (cgd) [Entry date 04/22/99]
☐	Runner	04/20/1999	75	REPLY by Plaintiff Cirrus Logic, Inc. in support of expedited motion for protective o information [52-1] [3:98-cv-02700] (cgd) [Entry date 04/22/99]
☐	Runner	04/20/1999	76	DECLARATION by Grant L. Kim on behalf of Plaintiff Cirrus Logic, Inc. re motion fo confidential information [52-1] [3:98-cv-02700] (cgd) [Entry date 04/22/99]

	Runner	04/20/1999	77	PROOF OF SERVICE by Cirrus Logic, Inc. of reply [75-1], declaration [76-1] [3:98- [Entry date 04/22/99]
	Runner	04/21/1999	78	NOTICE by Cirrus Logic, Inc. [61-1] order [3:98-cv-02700] (cgd) [Entry date 04/2
	Runner	04/21/1999	79	REPLY TO AMENDED COUNTERCLAIM [23-1] by Counter-defendant Cirrus Logic, Ir (cgd) [Entry date 04/23/99]
	Runner	04/21/1999	80	PROTECTIVE ORDER by Judge Susan Illston : (cc: all counsel) [3:98-cv-02700] (c 04/23/99]
	Runner	04/27/1999	81	NOTICE by Cirrus Logic, Inc. [80-1] order [3:98-cv-02700] (cgd) [Entry date 04/2
	Runner	04/28/1999	83	EXPEDITED MOTION before Judge Susan Illston by Plaintiff Cirrus Logic, Inc. for pr deposition. [3:98-cv-02700] (cgd) [Entry date 05/06/99]
	Runner	04/28/1999	84	DECLARATION by Mani Adeli on behalf of Plaintiff Cirrus Logic, Inc. re motion for p deposition [83-1] UNDER SEAL. [3:98-cv-02700] (cgd) [Entry date 05/06/99]
	Runner	05/03/1999	82	STIPULATION and ORDER by Judge Susan Illston : Re Briefing schedule for Cirrus' protective order re deposition. (cc: all counsel) [3:98-cv-02700] (cgd) [Entry date
	Runner	05/04/1999	85	OPPOSITION by defendant ATI Technologies Inc to plaintiff's motion for protective [83-1] UNDER SEAL. [3:98-cv-02700] (cgd) [Entry date 05/06/99]
	Runner	05/04/1999	86	DECLARATION by John W. Thornburgh on behalf of defendant ATI Technologies In UNDER SEAL [3:98-cv-02700] (cgd) [Entry date 05/06/99]
	Runner	05/04/1999	87	DECLARATION by Ruffin B. Cordell on behalf of defendant ATI Technologies Inc re UNDER SEAL [3:98-cv-02700] (cgd) [Entry date 05/06/99]
	Runner	05/04/1999	88	PROOF OF SERVICE by ATI Technologies Inc of opposition [85-1], declaration [86- [3:98-cv-02700] (cgd) [Entry date 05/07/99]
	Runner	05/06/1999	89	NOTICE by Cirrus Logic, Inc. [82-1] order [3:98-cv-02700] (cgd) [Entry date 05/1
	Runner	05/06/1999	90	REPLY by Plaintiff Cirrus Logic, Inc. to ATI's opposition to motion for protective ord 1] [3:98-cv-02700] (cgd) [Entry date 05/10/99]
	Runner	05/06/1999	91	DECLARATION by Grant L. Kim on behalf of Cirrus Logic, Inc. re motion reply [90- [3:98-cv-02700] (cgd) [Entry date 05/10/99]
	Runner	05/06/1999	92	PROOF OF SERVICE by Cirrus Logic, Inc. of motion reply [90-1], declaration [91-1 (cgd) [Entry date 05/10/99]
	Runner	05/12/1999	93	ORDER by Judge Susan Illston DENYING plaintiff's motion to shorten time on moti First Amended Complaint [49-1] [68-1]. Defendant shall file its opposition to moti by 6/4/99 ; plaintiff's reply by 6/11/99. Plaintiff's motion for leave to file an amen heard on 6/25/99 at 9:00a.m. (Date Entered: 5.13.99) (cc: all counsel) [3:98-cv- date 05/13/99]
	Runner	06/01/1999	94	ORDER Re: Discovery by Judge Susan Illston. (Date Entered: 6.1.99) (cc: all cour (cgd) [Entry date 06/02/99]
	Runner	06/02/1999	95	STIPULATION and ORDER by Judge Susan Illston to enlarge time for non-expert di Patent No. 5,598,525 and is extended to 8/13/99. (cc: all counsel) [3:98-cv-0270 06/07/99]
	Runner	06/02/1999	96	RESPONSE by defendant ATI Technologies Inc to Cirrus' amended claim chart und [47-1] UNDER SEAL. [3:98-cv-02700] (cgd) [Entry date 06/07/99]
	Runner	06/02/1999	97	RESPONSE by defendant ATI Technologies Inc to Cirrus' amended claim constructi Local Rule 16-10 [44-1] UNDER SEAL [3:98-cv-02700] (cgd) [Entry date 06/07/9
	Runner	06/02/1999	98	PROOF OF SERVICE by ATI Technologies Inc of response [96-1], response [97-1] (cgd) [Entry date 06/07/99]
	Runner	06/04/1999	99	OPPOSITION by defendant ATI Technologies Inc to Cirrus Logic's motion for leave Complaint [49-1] [3:98-cv-02700] (cgd) [Entry date 06/07/99]
	Runner	06/04/1999	100	PROOF OF SERVICE by ATI Technologies Inc of opposition [99-1] [3:98-cv-02700] 06/07/99]
	Runner	06/07/1999	101	NOTICE by Cirrus Logic, Inc. [95-1] order [3:98-cv-02700] (cgd)
	Runner	06/11/1999	102	REPLY by Cirrus Logic, Inc. in support of motion for leave to file First Amended Co cv-02700] (cgd) [Entry date 06/14/99]
	Runner	06/11/1999	103	MOTION before Judge Susan Illston by ATI Technologies Inc to bifurcate liability fr willfullness for discovery and trial. [3:98-cv-02700] (cgd) [Entry date 06/14/99]
	Runner	06/11/1999	104	MEMORANDUM IN SUPPORT by ATI Technologies Inc of motion to bifurcate liability willfullness for discovery and trial [103-1]. UNDER SEAL. [3:98-cv-02700] (cgd) [E [Edit date 06/17/99]
	Runner	06/11/1999	105	DECLARATION by Brian R. Nester on behalf of ATI Technologies Inc re motion to b damages and willfullness for discovery and trial [103-1] [3:98-cv-02700] (cgd) [E
	Runner	06/11/1999	106	PROOF OF SERVICE by ATI Technologies Inc of reply [102-1], motion to bifurcate and willfullness for discovery and trial [103-1], memorandum [104-1], declaration 02700] (cgd) [Entry date 06/14/99]
	Runner	06/15/1999	107	ORDER by Judge Susan Illston granting motion for protective order for confidential information by Ju

				(6.16.99) (cc: all counsel) [3:98-cv-02700] (cgd) [Entry date 06/16/99]
	Runner	06/16/1999	108	PROOF OF SERVICE by ATI Technologies Inc of motion to bifurcate liability from da willfullness for discovery and trial [103-1] [3:98-cv-02700] (cgd) [Entry date 06/1
	Runner	06/16/1999	109	(CORRECTED) MEMORANDUM by ATI Technologies Inc in support of motion to bifu damages and willfullness for discovery and trial.[103-1] UNDER SEAL. [3:98-cv-02 date 06/17/99]
	Runner	06/24/1999	110	STIPULATION and ORDER by Judge Susan Illston : continuing hearing on motion fo Amended Complaint [49-1] at 3:00p.m. on 7/6/99 by telephone. (cc: all counsel) (cgd) [Entry date 06/29/99]
	Runner	06/28/1999	111	NOTICE by Cirrus Logic, Inc. [110-1] order [3:98-cv-02700] (cgd) [Entry date 06/
	Runner	06/28/1999	112	STIPULATION and ORDER by Judge Susan Illston : extending time to file oppositio bifurcate. (cc: all counsel) [3:98-cv-02700] (cgd) [Entry date 07/01/99]
	Runner	06/30/1999	113	NOTICE by Cirrus Logic, Inc., [112-1] Scheduling order extending time to file oppo bifurcate. [3:98-cv-02700] (cgd) [Entry date 07/01/99]
	Runner	07/01/1999	114	STIPULATION and ORDER by Judge Susan Illston : extending time to file reply to C bifurcation. (cc: all counsel) [3:98-cv-02700] (cgd) [Entry date 07/06/99]
	Runner	07/02/1999	115	REPORTER'S TRANSCRIPT; Date of proceedings: April 1, 1999 (C/R: James Yeom (cgd) [Entry date 07/07/99]
	Runner	07/02/1999	116	OPPOSITION by Cirrus Logic, Inc. to Defendant's motion to bifurcate liability from willfullness for discovery and trial [103-1] UNDER SEAL. [3:98-cv-02700] (cgd) [E
	Runner	07/02/1999	117	DECLARATION by Seth E. Brown on behalf of Cirrus Logic, Inc. re opposition [116- (cgd) [Entry date 07/07/99]
	Runner	07/07/1999	118	JOINT CLAIM CONSTRUCTION STATEMENT [3:98-cv-02700] (cgd) [Entry date 07/
	Runner	07/08/1999	119	MINUTES: (C/R Roberta Rogers) (Hearing Date: 7/6/99) : Plaintiff's motion for le Amended Complaint [49-1] is held/submitted ; order to be prepared by Court. [3:: [Entry date 07/12/99]
	Runner	07/09/1999	120	CORRECTED DECLARATION by Seth E. Brown on behalf of Plaintiff Cirrus Logic, Inc 1] [3:98-cv-02700] (cgd) [Entry date 07/13/99]
	Runner	07/09/1999	121	REPLY by ATI Technologies Inc in support of its motion to bifurcate liability from da willfullness for discovery and trial [103-1] [3:98-cv-02700] (cgd) [Entry date 07/1
	Runner	07/09/1999	122	PROOF OF SERVICE by Counter-claimant ATI Technologies Inc of response [121-1] (ga) [Entry date 07/14/99]
	Runner	07/14/1999	123	OPENING CLAIM CONSTRUCTION BRIEF FILED by Cirrus Logic, Inc. UNDER SEAL. (cgd) [Entry date 07/16/99]
	Runner	07/14/1999	124	DECLARATION by Grant L. Kim on behalf of Cirrus Logic, Inc. re brief [123-1] UND 02700] (cgd) [Entry date 07/16/99]
	Runner	07/14/1999	125	DECLARATION by Richard F. Ferraro on behalf of Cirrus Logic, Inc. re brief [123-1] (cgd) [Entry date 07/16/99]
	Runner	07/14/1999	126	DECLARATION by Zacharia A. Higgins on behalf of Cirrus Logic, Inc. re brief [123-1 (cgd) [Entry date 07/16/99]
	Runner	07/15/1999	127	STIPULATION and ORDER by Judge Susan Illston regarding length of Claim Constr order dated 7/15/99 for specifics). (cc: all counsel) [3:98-cv-02700] (cgd) [Entry
	Runner	07/19/1999	128	NOTICE of International Trade Commission's affirmation of ALJ's determination of Technologies Inc [3:98-cv-02700] (cgd) [Entry date 07/20/99]
	Runner	07/19/1999	129	PROOF OF SERVICE by ATI Technologies Inc of notice [128-1] [3:98-cv-02700] (cg 07/20/99]
	Runner	07/19/1999	130	MINUTES: (C/R Lydia Radovich) (Hearing Date: 7/16/99) : ATI's motion to bifurc damages and willfullness for discovery and trial [103-1] is held/ submitted ; order Court. [3:98-cv-02700] (cgd) [Entry date 07/20/99]
	Runner	07/19/1999	131	ORDER by Judge Susan Illston DENYING motion for leave to file First Amended Co Entered: 7.21.99) (cc: all counsel) [3:98-cv-02700] (cgd) [Entry date 07/21/99]
	Runner	07/19/1999	132	ORDER by Judge Susan Illston GRANTING motion to bifurcate liability from damag discovery and trial [103-1]. Issues of liability will be tried separately from and bef willfull infringement and damages. Discovery on willful infringement and damages the initial trial. (Date Entered: 7.21.99) (cc: all counsel) [3:98-cv-02700] (cgd) [E
	Runner	07/28/1999	133	CLAIM CONSTRUCTION BRIEF filed by defendant ATI Technologies Inc UNDER SEA (cgd) [Entry date 07/29/99]
	Runner	07/28/1999	134	DECLARATION by Brian R. Nester on behalf of defendant ATI Technologies Inc re b SEAL. [3:98-cv-02700] (cgd) [Entry date 07/29/99]
	Runner	07/28/1999	135	DECLARATION by Bernard L. Peuto on behalf of defendant ATI Technologies Inc re cv-02700] (cgd) [Entry date 07/29/99]
	Runner	07/28/1999	136	PROOF OF SERVICE by ATI Technologies Inc of brief [133-1], declaration [134-1], [3:98-cv-02700] (cgd) [Entry date 07/29/99]
				REPLY BRIEF by Cirrus Logic, Inc. in support of claim construction statement [118-

☐	Runner	08/04/1999	137	[3:98-cv-02700] (cgd) [Entry date 08/09/99]
☐	Runner	08/04/1999	138	DECLARATION by Zachariah A. Higgins on behalf of Cirrus Logic, Inc. re claim con: [118-1] UNDER SEAL. [3:98-cv-02700] (cgd) [Entry date 08/09/99]
☐	Runner	08/04/1999	139	DECLARATION by Richard F. Ferraro on behalf of Cirrus Logic, Inc. re claim constr [118-1] [3:98-cv-02700] (cgd) [Entry date 08/09/99]
☐	Runner	08/04/1999	140	PROOF OF SERVICE by Cirrus Logic, Inc. of reply [137-1], declaration [138-1], dec [3:98-cv-02700] (cgd) [Entry date 08/09/99]
☐	Runner	08/05/1999	141	EX-PARTE APPLICATION before Judge Susan Illston by Plaintiff Cirrus Logic, Inc. to scheduling order [3:98-cv-02700] (cgd) [Entry date 08/09/99]
☐	Runner	08/10/1999	142	LETTER dated 8/5/99 from Grant L. Kim for Cirrus Logic, Inc. re a copy of the U.S. 5,598,525. UNDER SEAL. [3:98-cv-02700] (cgd) [Entry date 08/16/99]
☐	Runner	08/13/1999	143	LETTER dated 8/13/99 from Grant L. Kim re Cirrus' submitting a reexamination/rei the PTO, and will be moving to stay proceedings. [3:98-cv-02700] (cgd) [Entry da
☐	Runner	08/16/1999	144	EXPEDITED MOTION before Judge Susan Illston by Cirrus Logic, Inc. to stay pendi reexamination of the patent-in-suit. [3:98-cv-02700] (cgd) [Entry date 08/17/99]
☐	Runner	08/16/1999	145	DECLARATION by Grant L. Kim on behalf of Cirrus Logic, Inc. re motion to stay pe reexamination of the patent-in-suit. [144-1] [3:98-cv-02700] (cgd) [Entry date 08
☐	Runner	08/16/1999	146	LETTER dated 8/16/99 from John W. Thornburgh in response to the letter by Cirru 8/13/99. [3:98-cv-02700] (cgd) [Entry date 08/17/99]
☐	Runner	08/17/1999	147	SUPPLEMENTAL DECLARATION by Grant L. Kim on behalf of Cirrus Logic, Inc. re m reissuance and reexamination of the patent-in-suit. [144-1] [3:98-cv-02700] (cgd 08/18/99]
☐	Runner	08/18/1999	148	OPPOSITION by defendant ATI Technologies Inc to expedited motion to stay pendi reexamination of the patent-in-suit. [144-1] [3:98-cv-02700] (cgd) [Entry date 08
☐	Runner	08/18/1999	149	PROOF OF SERVICE by ATI Technologies Inc of opposition [148-1] [3:98-cv-0270C 08/19/99]
☐	Runner	08/27/1999	150	SUPPLEMENTAL BRIEF FILED by defendant ATI Technologies Inc regarding request SEAL. [3:98-cv-02700] (cgd) [Entry date 09/01/99]
☐	Runner	08/27/1999	151	DECLARATION by John W. Thornburgh on behalf of defendant ATI Technologies In UNDER SEAL. [3:98-cv-02700] (cgd) [Entry date 09/01/99]
☐	Runner	08/31/1999	153	LETTER dated 8/31/99 from Grant L. Kim re the supplemental briefing on Cirrus' m cv-02700] (cgd) [Entry date 09/08/99]
☐	Runner	09/01/1999	152	DECLARATION by John W. Thornburgh on behalf of defendant ATI Technologies In UNDER SEAL. [3:98-cv-02700] (cgd)
☐	Runner	09/01/1999	154	PROOF OF SERVICE by ATI Technologies Inc of declaration [152-1] [3:98-cv-0270 09/08/99]
☐	Runner	09/08/1999	155	SUPPLEMENTAL BRIEF FILED by Plaintiff Cirrus Logic, Inc. regarding motion to sta and reexamination of the patent-in-suit. [144-1] [3:98-cv-02700] (cgd) [Entry da
☐	Runner	09/08/1999	156	DECLARATION by Grant L. Kim on behalf of Plaintiff Cirrus Logic, Inc. re motion to reissuance and reexamination of the patent-in-suit. [144-1] [3:98-cv-02700] (cgd 09/10/99]
☐	Runner	09/08/1999	157	PROOF OF SERVICE by Cirrus Logic, Inc. of brief [155-1], declaration [156-1] [3:9 [Entry date 09/10/99]
☐	Runner	09/15/1999	158	RESPONSE by defendant ATI Technologies Inc to Cirrus' supplemental brief [155-1 (cgd) [Entry date 09/17/99]
☐	Runner	09/15/1999	159	PROOF OF SERVICE by ATI Technologies Inc of response [158-1] [3:98-cv-02700] 09/17/99]
☐	Runner	09/21/1999	160	LETTER dated 9/17/99 from Grant L. Kim re ATI's second supplemental brief as im disregard. [3:98-cv-02700] (cgd) [Entry date 09/22/99]
☐	Runner	11/05/1999	161	ORDER by Judge Susan Illston granting motion to stay pending reissuance and ree patent-in-suit. [144-1] to stay case (Date Entered: 11.8.99) (cc: all counsel) [3:9 [Entry date 11/08/99]
☐	Runner	11/05/1999	162	ORDER awarding costs by Judge Susan Illston. On 8/16/99, two days before a sch construction hearing, plaintiff Cirrus Logic, Inc. filed an expedited motion to stay t pending reissuance and reexamination of its patent. By separate order, this Court motion to stay. Accordingly, this Court determines that an award of $25,000 in co the unnecessary expense that ATI incurred, and hereby imposes these costs on Ci (Date Entered: 11.8.99) (cc: all counsel) [3:98-cv-02700] (cgd) [Entry date 11/0
☐	Runner	08/03/2000	163	ORDER Directing Status Report by Judge Susan Illston : The parties are hereby or status report, advising the Court of the status of the reissue and reexamination pr anticipated date when this case will be suitable for reopening. Status report is due Entered: 8.4.00) (cc: all counsel) [3:98-cv-02700] (cgd) [Entry date 08/04/00]
☐	Runner	08/21/2000	164	JOINT STATUS REPORT by Plaintiff, defendant [3:98-cv-02700] (cgd) [Entry date
☐	Runner	01/08/2001	165	ORDER by Judge Susan Illston parties directed to file status report on or before 1/ 1/19/01) (cc: all counsel) [3:98-cv-02700] (ab) [Entry date 01/19/01]

☐	Runner	01/19/2001	166	JOINT STATUS REPORT by Plaintiff, defendant [3:98-cv-02700] (cgd) [Entry date (
☐	Runner	10/03/2001	167	ORDER directing Status Report by Judge Susan Illston The parties are ordered to f is due 10/12/01 ; (Date Entered: 10/5/01) (cc: all counsel) [3:98-cv-02700] (ys) 10/05/01]
☐	Runner	10/12/2001	168	JOINT STATUS REPORT filed. [3:98-cv-02700] (ys) [Entry date 10/15/01]
☐	Runner	08/20/2002	169	ORDER by Judge Susan Illston : directing Status Report. The parties are ordered t report, advising the Court of the status of the reissue and reexamination proceedir anticipated date when this case will be suitable for reopening, on or before 8/30/0 8/20/02) (cc: all counsel) [3:98-cv-02700] (ys)
☐	Runner	08/30/2002	171	STATUS REPORT by Plaintiff Cirrus Logic, Inc., defendant ATI Technologies Inc [3: [Entry date 09/09/02]
☐	Runner	09/09/2002	170	NOTICE by Counter-claimant ATI Technologies Inc, defendant ATI Technologies In thornburgh of change of address [3:98-cv-02700] (ys)
☐	Runner	07/29/2003	--	RECEIVED sbustitution of attorneys to the law firm of White & Case LLP submitted Logic, Inc. [3:98-cv-02700] (ys) [Entry date 07/31/03]
☐	Runner	07/29/2003	172	NOTICE OF MOTION AND MOTION before Judge Susan Illston by Plaintiff Cirrus Lo with Notice set for 9/12/03 at 9:00 a.m. [3:98-cv-02700] (ys) [Entry date 07/31/(
☐	Runner	07/29/2003	173	DECLARATION by Warren S. Heit on behalf of Plaintiff Cirrus Logic, Inc. re motion [3:98-cv-02700] (ys) [Entry date 07/31/03]
☐	Runner	07/29/2003	--	RECEIVED Proposed Order (Plaintiff Cirrus Logic, Inc.) re: motion to dismiss [172 (ys) [Entry date 07/31/03]
☐	Runner	08/11/2003	174	ORDER by Judge Susan Illston withdrawing attorney Seth E. Brown for Cirrus Logi Russell B. Hill for Cirrus Logic, Inc., attorney Michael A. Jacobs for Cirrus Logic, In attorney Warren S. Heit (Date Entered: 8/12/03) (cc: all counsel) [3:98-cv-0270(08/12/03]
☐	Runner	08/22/2003	175	RESPONSE by defendant ATI Technologies Inc re motion to dismiss [172-1] [3:98-
☐	Runner	08/28/2003	--	RECEIVED Joint Stipulation and proposed order to continue the hearing on Cirrus L dismiss submitted by Plaintiff Cirrus Logic, Inc. [3:98-cv-02700] (ys) [Entry date (
☐	Runner	09/03/2003	176	JOINT STIPULATION and ORDER by Judge Susan Illston : setting hearing on motio 10/24/03, the deadline for Cirrus Logic to file its reply brief is extended to 10/10/([3:98-cv-02700] (ys) [Entry date 09/04/03]
☐	Runner	09/26/2003	--	RECEIVED Joint stipulation of voluntary dismissal with prejudice submitted by Plair [3:98-cv-02700] (ys) [Entry date 09/29/03]
☐	Runner	09/30/2003	177	JOINT STIPULATION and ORDER of Voluntary Dismissal with Prejudice by Judge St dismissing case ; appeal filing ddl 10/30/03 (cc: all counsel) [3:98-cv-02700] (ys)
☐	Runner	10/20/2003	178	MAIL [177-2] addressed to Brian R. Nester, Esq. returned from Post Office [3:98-c date 10/22/03]
☐	Runner	10/20/2003	179	MAIL [178-1] addressed to Linda Liu Kordziel, Esq. returned from Post Office [3:9 [Entry date 10/22/03]
☐	Runner	10/20/2003	180	MAIL [177-1] addressed to Ruffin B. Cordell, Esq. returned from Post Office [3:98- date 10/22/03]
☐	Runner	10/20/2003	181	MAIL [177-1] addressed to Michael J. McKeon, Esq. returned from Post Office [3:9 [Entry date 10/22/03]

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376919 (08) 5598525 January 28, 1997

UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT

5598525

January 28, 1997

Apparatus, systems and methods for controlling graphics and video data in multimedia data processing and display systems

REEXAM-LITIGATE:

NOTICE OF LITIGATION

NOTICE OF LITIGATION Cirrus Logic, Inc. v. ATI Technologies, Inc., Filed Jul. 8, 1998, D.C. N.D. California, Doc. No. 98-2700 SI

NOTICE OF LITIGATION

NOTICE OF LITIGATION Reexamination Requested Aug. 13, 1999 by owner, Reexamination No. 90/005,473 (O.G. Nov. 9, 1999) Ex. Gp.: 2776

INVENTOR: Nally, Robert M. - Plano, Texas, United States (US); Schafer, John C. - Wylie, Texas, United States (US)

CERT-CORRECTION: May 11, 1999 - a Certificate of Correction was issued for this patent
December 2, 1997 - a Certificate of Correction was issued for this patent

APPL-NO: 376919 (08)

FILED-DATE: January 23, 1995

GRANTED-DATE: January 28, 1997

ASSIGNEE-AT-ISSUE: Cirrus Logic, Inc., Fremont, California, United States (US), 02

ASSIGNEE-AFTER-ISSUE: January 23, 1995 - ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS)., CIRRUS LOGIC, INC. 3100 WEST WARREN AVENUE FREMONT CALIFORNIA 94538, Reel and Frame Number: 07326/0692
August 29, 1996 - SECURITY AGREEMENT, BANK OF AMERICA NATIONAL TRUST & SAVINGS ASSOCIATION AS AGENT 1455 MARKET STREET SAN FRANCISCO CALIFORNIA 94103, Reel and Frame Number: 08113/0001
November 10, 2003 - ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS), NVIDIA INTERNATIONAL, INC. C/O PRICEWATERHOUSECOOPERS (CORPORATE SERVICE LTD) THE FINANCIAL SERVICES CENTER ERIN COURT BISHOP'S

COURT HILL ATTENTION CLAUDIA CLARK ST. MICHAEL BARBADOS WISCONSIN, Reel and Frame Number: 14646/0167

LEGAL-REP: Fulbright & Jaworski LP. - Dallas Office

PUB-TYPE: January 28, 1997 - Utility Patent having no previously published pre-grant publication (A)

PUB-COUNTRY: United States (US)

US-MAIN-CL: 345#546

US-ADDL-CL: 345#505, 345#548, 345#558, 345#634

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IPC-MAIN-CL: 6G 06F015#0

PRIM-EXMR: Powell, Mark R.

ASST-EXMR: Chauhan, U.

REF-CITED:
04991122, February, 1991, Sanders, United States (US), 395131
05218432, June, 1993, Wakeland, United States (US), 346590
05229852, July, 1993, Maietta et al., United States (US), 348441
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05406306, April, 1995, Siann et al., United States (US), 345115

NON-PATENT LITERATURE:
Steve Undy "A Low-Cost Graphics & Multimedia Workstation Chip Set" IEEE Micro. Apr. 1994, pp. 10-82.
Bill Snyder "The Cirrus Scar" PC Week, Oct. 1994, v11, n42, pA1 (3).
James Turley "Brooktire reveals Multimedia Plans;" Microprocessor Reprot. Dec. 1994, v8, n16, p. 19 (1).
Dave Bursky "Acceleration puts the `snap` into graphics" Electronic Design, Jul. 1994, v42, n15, p55(7).
Anthony Cataldo "WD, Cirrus Show Video Playback ICs" Electronic News, Oct. 1994, v40, n2035, p66(1).
Edge: Work-Group Computing Report, Oct. 1994, v5, n228 p15(1) , Edge Publishing.
Jeff Mace "Mainstream graphics accelerators rush power" PC Magazine, Dec. 1994, v13, n21, p239 (17).

CORE TERMS: video, graphics, pipeline, circuitry, window, display, pixel, buffer, memory, screen, color, overlay, input, register, multiplexer, controller, backend, on-screen, bit, off-screen, back-end, interface, rastered, counter, processing, stored, bus, screen memory, playback, raster

ENGLISH-ABST:

A graphics and video controller 105 is provided which includes a dual aperture interface 206 for receiving words of graphics and video pixel data, each word of such data associated with an address directing that word to be processed as either graphics or video data. Circuitry 200, 201, 202, 207, 208 is provided for writing a word of the pixel data

received from the interface 206 to a one of the on- and off-screen memory areas corresponding to the address associated with the received word. Circuitry 201, 202 is provided for selectively retrieving graphics and video data from the on-screen and off-screen memory areas. A first pipeline 205 is provided for processing data received from the on-screen area of frame buffer 107 while a second pipeline 204 is provided for processing data retrieved from the off-screen area of the frame buffer.

NO-OF-CLAIMS: 47

EXMPL-CLAIM: 13

NO-DRWNG-PP: 4

SUMMARY:

TECHNICAL FIELD OF THE INVENTION

The present invention relates in general to multimedia processing and display systems and in particular to apparatus, systems and methods for controlling graphics and video data overlay in multimedia processing and display systems.

CROSS-REFERENCE TO RELATED APPLICATIONS

The following copending and coassigned United States patent applications contain related information and are incorporated herein by reference:

U.S. patent application Ser. No. 08/098,846 (Attorney's Docket No. P3510-P11US), entitled "System And Method For The Mixing Of Graphics And Video Signals," and filed Jul. 29, 1993; and

U.S. patent application Ser. No. 08/223,845 (Attorney's Docket No. P3510-P21US), entitled "Apparatus, Systems And Methods For Processing Video Data In Conjunction With A Multi-Format Frame Buffer," and filed Apr. 6, 1994.

BACKGROUND OF THE INVENTION

As multimedia information processing systems increase in popularity, system designers must consider new techniques for controlling the processing and display of data simultaneously generated by multiple sources. In particular, there has been substantial demand for processing systems which have the capability of concurrently displaying both video and graphics data on a single display screen. The development of such systems presents a number of design challenges, not only because the format differences between graphics and video data must be accounted for, but also because of end user driven requirements that these systems allow for flexible manipulation of the data on the display screen.

One particular technique for simultaneously displaying video and graphics data on a single display screen involves the generation of "windows." In this case, a stream of data from a selected source is used to generate a display within a particular region or "window" of the display screen to the exclusion of any non-selected data streams defining a display or part of a display corresponding to the same region of the screen. The selected data stream generating the display window "overlays" or "occludes" the data from the nonselected data streams which lie "behind" the displayed data. In one instance, the overall content and appearance of the display screen is defined by graphics data and one or more "video windows" generated by data from a video source occlude a corresponding region of that graphics data. In other instances, a video display or window may be occluded or overlaid by graphics data or even another video window.

In the multimedia environment, the windowing described above yields substantial

advantages. Among other things, the user can typically change the size and location on the display screen of a given window to flexibly manipulate the content and appearance of the data being displayed. For example, in the case of combined graphics and video, the user can advantageously create custom composite visual displays by combining multiple video and graphics data streams in windowing environment.

In order to efficiently control windows in a multimedia environment efficient frame buffer management is required. Specifically, a frame buffer control scheme must be developed which allows for the efficient storage and retrieval of multiple types of data, such as video data and graphics data. To be cost competitive as well as functionally efficient, such a scheme should minimize the number of memory devices and the amount of control circuitry required and should insure that data flow to the display is subjected to minimal delay notwithstanding data type.

One of the major difficulties in managing video in a combined video and graphics windowing environment results from the fact that the video data being received and displayed are constantly being updated, typically at a rate of thirty frames per second. In contrast, the graphics data are normally generated once to define the graphics display and then remain static until the system CPU change that graphics display. Thus, the occlusion (overlay) of video data with graphics data requires that the static graphics data "in front of" the video data not be destroyed each time the video window is updated. A second concern with windowing systems operating on both video and graphics data is the formatting differences between the video and graphics data themselves since video is typically digitized into a YUV color space while graphics is digitized into an RGB color space. Hence, any combination video and graphics windowing system must have the capability of efficiently handling data within both the YUV and RGB formats.

Thus, due to the advantages of windowing, the need has arisen for efficient and cost effective windowing control circuitry. Such windowing circuitry should allow for the simultaneous processing of data received from multiple sources and in multiple formats. In particular, such windowing control circuitry should be capable of efficiently and inexpensively controlling the occlusion and/or overlay of video and graphics data in a windowing environment.

SUMMARY OF THE INVENTION

The principles of the present invention in general provide for the flexible control of graphics and video data in a display control environment. In particular, an entire frame of video data, graphics data, or a combination of both, may be stored in on-screen memory and rastered out with the generation of the corresponding display screen. A window of graphics or video data can then be stored in off-screen memory and retrieved when the raster scan generating the display reaches the desired position on the display for the video window. The window of data from off- screen memory can then be overlayed over the data being rastered out of the on-screen memory under one of three conditions. In a first mode, pixels from the off-screen memory are rastered only when the raster scan has reached the position on the display selected for the window. In a second mode, a window of data is rastered from the off- screen memory when the display raster scan has reached the display window position and graphics data being rastered from the on-screen memory matches a color key. In a third mode, the window data is rastered out of the off-screen memory when the data being output from the on- screen memory matches the color key, notwithstanding the position of the raster scan.

According to a first embodiment of the present invention, a graphics and video controller is provided which includes a dual aperture interface, each word associated with an address to a selected one of on- screen and off- screen areas of an associated unified frame buffer as either graphics or video pixel data. Circuitry is provided for writing a word of the pixel data received by the interface to a one of the on- screen and off- screen memory areas corresponding to the address associated with the received word. Circuitry is also included for selectively retrieving graphics and video data from the on-screen and off- screen memory areas. A first pipeline is provided for processing graphics data

retrieved from the frame buffer and a second pipeline is provided for video processing data retrieved from the frame buffer.

According to a second embodiment of the present invention, a controller is provided which includes a dual aperture port for receiving video and graphics data, each word of the data received with an address associated directing the word to be processed as either graphics or video data and off-screen memory spaces of a frame buffer. A second port is included for receiving real- time video data. Circuitry is provided for generating an address associated with a selected one of the memory spaces for each word of received real-time video data. Circuitry is included for writing selectively the words into the on-screen and off- screen memory spaces of the frame buffer. Circuitry is also provided for selectively retrieving the words of data from the on-screen and off- screen spaces as data is rastered for driving a display. A graphics backend pipeline processes ones of the graphics words of data retrieved from the frame buffer. A video backend pipeline is provided for processing ones of the video words of data retrieved from the frame buffer, the circuitry for retrieving always rastering a stream of graphics data from the frame buffer to the graphics pipeline and rastering video data to the video backend pipeline when a display raster scan reaches a display position of a video window. An output selector is included for selecting for output between words of data output from the graphics backend pipeline and words of data output from the video backend pipeline.

According a third embodiment of the present invention, a display system is provided which includes first and second parallel backend pipelines. A multi-format frame buffer memory is included having on- screen and off- screen memories each operable to simultaneously store data in graphics and video formats. A dual aperture port is provided for receiving both graphics and video data as directed by an address associated with each word of data received. Circuitry for writing is included for writing a word of video or graphics data into a selected one of the on-screen and off-screen areas of the multi-frame buffer. Memory control circuitry controls the transfer of data between the first and second back-end pipelines and the frame buffer. The system further includes a display unit and overlay control circuitry for selecting for output to the display unit between data provided by the first backend pipeline and data provided by the second backend pipeline.

A fourth embodiment of the present invention comprises a display data processing system which includes circuitry for writing data into an on- screen space of a frame buffer and circuitry for writing data into an off- screen space of the frame buffer. A video pipeline is provided for processing video data output from a selected one of the on- screen and off-screen spaces. The video pipeline includes a first first- in/first- out memory for receiving selected pixel data from the selected space. The video pipeline also includes a second first-in/first-out memory disposed in parallel to the first first-in/first-out memory for receiving other selected data from the selected space in the frame buffer. An interpolator is provided as part of the video pipeline for generating additional data by interpolating data output from the first and second first-in/first-out memories. A graphics pipeline is disposed in parallel to the video pipeline for processing graphics data output from a selected one of the on-screen and off-screen spaces. Finally, an output selector is provided for selecting between data output from the video pipeline and data output from the graphics pipeline.

The principles of the present invention allow for the construction of circuits and systems with substantial advantages over the prior art. Among other things, the principles of the present invention allow both graphics and video data to be stored in a single unified frame buffer and retrieved therefrom in a number of different ways. For example, a combination of graphics and video data may be stored in the on-screen memory and simply rastered out during screen refresh. In another case, an entire screen of graphics or video data may be stored in the on-screen memory while a window of graphics or video data is stored in the off- screen portion of memory. The window data can then be rastered out to selectively overlay a portion of the data being rastered out of the on- screen memory. The overlay may be controlled by either window display position with a match of the on-screen data being rastered out and a color key, or both.

The embodiments of the present invention provide for the efficient and inexpensive overlay of video and graphics data in a windowing environment. In particular, the use of color comparison to determine the overlay of data in a window region eliminates the need for precise x- and y-position data for the location of that window and allows for video cropping to be performed. Further, the use of graphics data to control overlay provides substantial advantages in that graphics data is less subject to the graininess and noise problems often found with video data. Further, the user is given total control of overlay operations when keying on graphics data because the graphics data is computer generated, whereas the video data is captured data.

DRWDESC:

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a top level functional block diagram of a multi-media processing and display system embodying the principles of the present invention;

FIG. 2 is a more detailed functional block diagram of the VGA controller depicted in FIG. 1;

FIG. 3 is an expanded functional block diagram of portions of the controller of FIG. 2 with emphasis on the overlay control features;

FIG. 4A is a detailed functional block diagram of a first embodiment of the color comparison circuitry of FIG. 3;

FIG. 4B is a detailed functional block diagram of a second embodiment of the color comparison circuitry of FIG. 3; and

FIG. 5 is a detailed functional block diagram of a selected one of the video window position control circuits depicted in FIG. 3.

DETDESC:

DESCRIPTION OF THE INVENTION

FIG. 1 is a high level functional block diagram of a multi- media processing and display system 100 operable to process and simultaneously display on a single display screen both graphics and video data according to the principles of the present invention. Display system 100 includes a central processing unit (CPU) 101 which controls the overall operation of system 100 and generates graphics data defining graphics images to be displayed. CPU 101 communicates with the remainder of the system discussed below via a local bus 103. System 100 also includes a real-time video data source 104. A real time video stream may be presented to the system VGA controller 105 in one of two ways. First, video data source 104 may be coupled to local bus 103 and a video data stream introduced through dual aperture addresses. In this case, video source 104 will directly address the system frame buffer 107. Second, video source 104 may be coupled directly to VGA controller 105 via a dedicated bus 109 or "video port." In this instance, VGA controller 105 generates the required addresses into frame buffer 107. Real-time video source 104 may be, for example, a CD ROM unit, a laser disk unit, a videotape unit, television cable outlet or other video data source outputting video data in a YUV format. CPU 101 operates in conjunction with a system memory 108 which stores graphics and video data on a real- time basis. System memory 108 may be for example random access memory (RAM), floppy disk, hard disk or other type of storage device.

A VGA controller 105 embodying the principles of the present invention is also coupled to local bus 103. VGA controller 105 will be discussed in detail below; however, VGA controller 105 generally interfaces CPU 101 and video source 104 with a display unit 106 and a multiformat system frame buffer 107. Frame buffer memory 107 provides temporary storage of the graphics and video data during processing prior to display on display unit 106. According to the principles of the present invention, VGA controller is operable in selected modes to store graphics and video data together in frame buffer 107 in their native formats. In a preferred embodiment, the frame buffer area is partitioned into on-screen memory and off-screen memory. Frame buffer 107 is also a "unified" memory in which video or graphics data can be stored in either the on-screen or off-screen areas. In the preferred embodiment, display unit 106 is a conventional raster scan display device and frame buffer 107 is constructed from dynamic random access memory devices (DRAMs).

FIG. 2 is a more detailed functional block diagram of VGA controller 105. The primary circuitry blocks of VGA controller 105 include video front- end video pipeline 200, memory (frame buffer) control circuitry 201, CRT/window control circuitry 202, video window control registers 203, video back-end pipeline 204 and graphics back-end pipeline 205. VGA controller 105 further includes a CPU interface 206 for exchanging instructions and data via a PCI or VL bus, such as local bus 103 in system 100, with CPU 101. A write buffer 207 and conventional graphics controller 208 allow CPU 101 to directly control data within frame buffer 107 via memory control circuitry 201.

In the preferred embodiment of system 100, CPU 101 can write video data and/or read and write graphics data to frame buffer 107 via CPU interface 206. In particular, CPU 101 can direct each pixel to the frame buffer using one of two maps depending on whether that pixel is a video pixel or a graphics pixel. In the preferred embodiment, each word of pixel data ("pixel") is associated with one of two addresses, one which directs interpolation of the pixel as a video pixel through video front- end pipeline 200 and the other which directs interpolation of the pixel as a graphics pixel through write buffer 207 and graphics controller 208. As a consequence, either video or graphics pixel data can then be input to CPU interface 206 from the PCI/VI bus through a single "dual aperture" port as a function of the selected address.

Data which is input through the video port 211 address-free. In this case, video window controls 213 generates the required addresses to either the on-screen memory area or the off-screen memory as a function of display location for the video window. In the preferred embodiment, window controls 213 generate addresses using the same video control registers 203 used to control retrieval of the video in the back-end pipeline (i.e., the screen x and y position registers 500 and 501 discussed below in conjunction with FIG. 5) . When data is being received through both the CPU interface 206 and the VPORT 211 simultaneously, the data is interleaved into memory with the two write buffers 207 and 217 buffering the data such that neither stream is interrupted or forced into a wait state at the source component (i.e., bus 103 or video source 104).

It should be noted at this point that frame buffer 107 includes at least two different data areas or spaces to which data can be directed by the given address (either CPU 103 or controls 213 generated. Each space can simultaneously store graphics or video data depending on the selected display configuration. The on-screen area corresponds to the display screen; each pixel rastered out of a given pixel location in the on- screen area defines a corresponding screen pixel. The off-screen area is used to store data defining a window for selectively overlaying the data from the on-screen memory, fonts and other data necessary by controller 105. Further, as will discussed further below, both graphics and video data may be rastered from frame buffer 107 and passed through video backend pipeline 204 while only graphics data is ever passed through graphics backend pipeline 205.

According to the principles of the present invention, there are alternate ways of storing and retrieving graphics and video data from unified frame buffer 107.

For example, CPU 103 may write a static graphics background into part of the on-screen memory with the remaining "window" in the on- screen memory area filled with playback video data. "Playback" video data can be either (1) live video data input from the VPORT; (2) YUV (video) data written through interface 206 by CPU 103; or (3) true color (5:5:5, 5:6:5, or 8:8:8) RGB graphics data (for example animation graphics data) written in through either the VPORT or interface 206. Similarly, a playback video background and a window of graphics data may be written into the on-screen area. In each of these cases, the data is rastered out as the display is without overlay; the video playback data is passed through the video playback data is passed through the video backend pipeline 204 as a function of display position by controls 202 and the graphics data passed through the graphics backend pipeline 250.

Windows of data retrieved from the off-screen memory can be retrieved and used to occlude a portion of the data being rastered out of the on- screen memory. For example, a window of playback data can be stored in the off- screen memory and a frame of static graphics data (either true color data or indices to CLUT 234) stored in the on-screen memory. In this case, the static graphics are rastered out of the on- screen memory without interruption and passed through the graphics backend pipeline 205. The window of data in the off- screen memory is rastered out only when the display position for the window has been reached .by the display raster and is passed through video backend pipeline 204. As discussed below, data from the video backend pipeline 204 can then be used to selectively occlude (overlay) the data being output from the graphics backend pipeline 205. A window of static graphics data (true color or indices to the CLUT 234) can be stored in off-screen memory and used of overlay playback video from the on-screen memory, the playback video data is passed through the video backend pipeline 204 and the window of static graphics data is passed through the graphics backend pipeline 205.

Bit block transfer (BitBLT) circuitry 209 is provided to allow blocks of graphics data within frame buffer 107 to be transferred, such as when a window of graphics data is moved on the display screen by a mouse. Digital-to- analog converter (DAC) circuitry 210 provides the requisite analog signals for driving display 106 in response to the receipt of either video data from video back-end pipeline 204 or graphics data from back-end pipe line 208.

In implementing the operations discussed above, video front-end pipeline 200 can receive data from two mutually exclusive input paths. First, in the "playback mode," playback (non-real time) data may be received via the PCI bus through CPU interface 206. Second, in the "overlay emulation mode" either real-time or playback video may be received through the video port interface 211 (in system 100 video port interface 211 is coupled to bus 109 when real-time data is being received) . The selection of video from the PCI bus or video from video port interface 211 is controlled by a multiplexer 212 under the control of bits stored in a video front-end pipeline control register within video control registers 203. In the playback mode, either CPU 101 or a PCI bus master controlling the PCI bus provides the frame buffer addresses allowing video front-end pipeline 200 to map data into the frame buffer separate and apart from the graphics data. In the overlay emulation mode, overlay input window controls 213 receives framing signals such as VSYNC and HSYNC, tracks these sync signals with counters to determine the start of each new frame and each new line, generates the required addresses for the real-time video to the frame buffer space using video window position data received from window controls 222 (as discussed above, in the preferred embodiment, video data is always retrieved from either the on- screen on off-screen memory and passed through video back-end pipeline 204 as a function of display position) and thus the position data from controls 222 is used to both write data to memory and retrieve data therefrom). In general, overlay input video control windows are controlled by the same registers which control the back-end video pipeline 204, although the requisite counters and comparators are located internal to overlay input video control circuitry 213.

Video front-end pipeline 200 also includes encoding circuitry 214 that is operable to truncate 16-bit YUV 422 data into an 8-bit format and then pack four such 8-bit encoded

words into a single 32-bit word which is then written into the video frame buffer space of frame buffer 105. Conversion circuitry 215 is operable to convert RGB 555 data received from either the CPU interface 206 and the PCI bus or VPORT I/F 211 into YCrCb (YUV) data prior to encoding by encoding circuitry 214. Conversion circuitry 215 allows graphics data (for example in a 5:5:5 or 5:6:5 format) to be introduced through the VPORT or graphics data to be converted, packed and stored in a YUV format in the off-screen memory space by CPU 101. For a more complete description of encoder 214 and the associated decoder 225 of video pipeline 204, reference is now made to incorporated copending coassigned application Ser. No. 08/223,845. The selection and control of the encoding circuitry 214 and conversion circuitry 215 is implemented through multiplexing circuitries 212 and 216, each of which are controlled by bits in the video control registers. Finally, video front-end pipeline 200 includes a write buffer/FIFO 217 which in one embodiment acts as a write buffer and in an alternate embodiment acts as a FIFO for the video backend pipeline 204. In embodiments where buffer 217 acts as a write buffer for then Y, zooming on the back-end, as discussed below is by replication. In embodiments where buffer 217 operates as a FIFO, then the VPORT and front and end color conversion by converter circuitry 215 are not used for writing data to frame buffer 107.

Memory control circuitry 201 includes an arbiter 218 and a memory interface 219. Arbiter 218 prioritizes and sequences requests for access to frame buffer 107 received from video front-end pipeline 200, graphics controller 208 and bit block transfer circuitry 209. Arbiter 218 further sequences each of these requests with the refresh of the display screen of display 106 under the control of CRT controller 202. Memory interface 219 controls the exchange of addresses, data, and control signals (such as RAS, CAS and read/write enable) to and from frame buffer 107.

CRT control/video window control circuitry 202 includes the CRT controller 220, window arbiter 221, and video display window controls 222. CRT controller 202 controls the refresh of the screen of display 106 and in particular the rastering of data from frame buffer 107 to display unit 107 through DAC 210. In the preferred embodiment, CRT controller 220, through arbiter 218 and memory interface 219, maintains a constant stream of graphics data into graphics backend pipeline 205 from memory; video or playback graphics data is rastered out only when a window has been reached by the display raster as determined by display position controls of window controls 222 (see FIGS. 3 and 5 and accompanying text) and CRT controller 220. As will be discussed in further detail below, the display of windows within the display according to the principles of the present invention is controlled in part by circuitry 202.

Video back-end pipeline 204 receives a window of graphics video data defining a display window from the on-screen or off-screen spaces in frame buffer 107 through a pair of first-in/first-out memories 223 and 217 (in embodiments where buffer 217 is acting as FIFO B). In the preferred embodiment, each FIFO receives the data for every other display line of data being generated for display on the display screen. For example, for a pair of adjacent lines n-1 and n+1 in memory (although not necessarily adjacent on the display) for the display window, FIFO 223 receives the data defining window display line n-1 while FIFO 224 receives the data defining window display line n+1. When buffer 217 is used as FIFO B, writes through video front end pipeline 200 are made through write buffer I 207 and multiplexer 235. Alternatively, if buffer 217 is used as write buffer II, then FIFO B is not implemented and only a single stream is processed by video back-end pipeline 204 (no Y interpolation is performed and Y expansion is by replication). As will be discussed further below (assuming both FIFO A and FIFO B are being used), one or more display lines, which falls between line n-1 and line n+1, may be selectively generated by interpolation. Decoder circuitry 225 receives two 32-bit packed words (as encoded by encoder 214), one from each adjacent scan line in memory, from FIFOs 223 and 217. Each 32-bit word, which represents four YCrCb pixels, is expanded and error diffused by decoder 225 into four 16-bit YCrCb pixels. In modes where video data is stored in the frame buffer in standard 555 RGB or 16 YCrCb data formats, decoder block 225 is bypassed.

Back end video pipeline 204 further includes a Y interpolator 226 and X interpolator 227.

In the preferred embodiment, during Y zooming (expansion) Y interpolator 226 accepts two vertically adjacent 16-bit RGB or YCrCb pixels from the decoder 225 and calculates one or more resampled output pixels using a four subpixel granularity. X interpolator 227 during X zooming (expansion) accepts horizontally adjacent pixels from the Y interpolator 226 and calculates one or more resampled output pixels using a four subpixel granularity. For data expansion using line replication, Y interpolator 226 is bypassed. Y interpolator 226 and X interpolator 227 allow for the resizing of a video display window being generated from one to four times.

The output of X interpolator 227 is passed to a color converter 228 which converts the YCrCb data into RGB data for delivery to output multiplexer 304. To reiterate, if graphics data is passed through video pipeline converter 228 is not used.

Back-end video circuitry 204 further includes pipeline control circuitry 229, overlay control circuitry 230 and output multiplexer 231. Pipeline control circuitry 239 controls the reading of data from video FIFOs 223 and 217, controls the generation of interpolation coefficients for use by X and Y interpolators 226 and 227 to resize the video window being pipelined, and times the transfer of data through the pipeline. Overlay control circuitry 230 along with control circuitry 202, controls the output of data through output multiplexer 231, including the overlay of the video window over the graphics data output through the graphics back-end pipeline 205. A pixel doubler is provided to double the number of pixels being generated such that a 1280*1024 display can be driven.

Graphics back-end pipeline 205 includes a first-in/first-out memory 232, attribute controller 233, and color look-up table 234. Each 32-bit word output from graphics FIFO 232 is serialized into either 8- bit, 16- bit or 24- bit words. The 8-bit words, typically composed of an ASCII code and an attribute code, are sent to attribute controller 233. When 16-bit and 24-bit words, which are typically color data, are serialized, those words are sent directly overlay controls 230. Attribute controller 233 performs such tasks as blinking and underlining operations in text modes. The eight bits output from attribute controller 233 are pseudo-color pixels used to index CLUT 234. CLUT 234 preferably outputs 24-bit words of pixel data to output multiplexer 231 with each index. When video data is being pipelined through graphics backend pipeline 205 from the on- screen memory, CLUT 234 is bypassed.

The eight bit pseudo-color pixels are output from attribute controller 233 are also sent to overlay controls 230. In the preferred embodiment, data is continuously pipelined from on-screen memory through graphics back-end pipeline 205 to the inputs of output multiplexer 231. Window data from off-screen memory however is only retrieved from memory and pipelined through video backend pipeline 204 when a window is being displayed. In other words, when a window has been reached, as determined by control bits set by CPU 101 in VW control registers 222, video window display controls 222 generate addresses to retrieve the corresponding data from the off-screen memory space of frame buffer 107. Preferably, video FIFOs 223 and 224 are filled before the raster scan actually reaches the display window such that the initial pixel data is available immediately once the window has been reached. In order to insure that graphics memory data continues to be provided to graphics back-end pipeline 205, video window display controls 222 "steal" page cycles between page accesses to the graphics memory. It should be noted that once the window has been reached the frequency of cycles used to retrieve window data increases over the number used to fill the video FIFOs when outside a window. When the frequency of window page accesses increases, video window display controls 222/arbiter 221 preferably "steal" cycles from page cycles being used to write data into the frame buffer.

FIG. 3 is a more detailed functional block diagram emphasizing the circuitry controlling the overlay of data from graphics pipeline 205 with window data from video pipeline 204. As discussed briefly above, the inputs to output multiplexer 231 are data from video back-end pipeline 204 (pixel doubler 237), 16 or 24-bit color data directly from graphics back-end pipeline 205 serializer 236 and 24-bit color data from the color look-up table 234. The output of data to DAC 210 through output multiplexer 231 is controlled by a

latch 301 clocked by the video clock (VCLK). The remaining circuitry shown in FIG. 3, which will be discussed in further detail below, provide the necessary control signals to the control inputs of output multiplexer 231 to select between the video and graphics pipelines.

The graphics pseudo-pixels output from attribute controller 233 and the 16-bit or 24-bit graphics or video data output directly from serializer 236 are provided to the inputs of color comparison circuitry 302. Also input to color comparison circuit 302 are 16 or 24-bit overlay color key bits stored in overlay color key register 303. Overlay color key register 303 resides within the address space of, and is loaded by, CPU 101. Depending on the mode, color comparison circuitry 302 compares selected bits from the overlay color key register 303 with either the 8 bits indexing look-up table 234 in the color look-up table mode (pseudo- color mode) or the 16-bits (24-bits in the alternate embodiment) passed directly from serializer 236. It should be noted that in the illustrated embodiment, overlay color key register 303 holds 24-bits of overlay color key bits, eight each for red, green, and blue/index comparisons. The specific overlay color key bits compared with the input graphics data are provided in Table I:

MODE OVERLAY COLOR KEY BITS COMPARED

CLUT -- -- -- -- Blue/Index

Index < 7:0 >

5:5:5 Red < 4:0 > Green < 4:0 > Blue < 4:0 >

5:6:5 Red < 4:0 > Green < 5:0 > Blue < 4:0 >

8:8:8 Red < 7:0 > Green < 7:0 > Blue < 7:0 >

As shown in FIG. 4A, a first embodiment of color comparison circuitry 303 performs the comparisons set forth in Table I as a set of XNOR operations in series with an AND operation. FIG. 4A depicts first comparison circuitry 400 for comparing the 8-bits of graphics pixels received in the look-up table mode from attribute controller 233 with the 8-bit blue/index overlay key bits being held in overlay key register 303. Second comparison circuitry 401, performs the required comparisons of Table I for the 16-bit data or 24-bit received from serializer 236, in, either a 5:5:5, 5:6:5, or 8:8:8 format. An overlay register 402 includes a bit loaded by CPU 101 which is used by a selector 403, depending on the mode, to select for output, either the result of the comparisons being made by comparison circuitry 400 in the color look-up table mode or the results of the comparisons being made by comparison circuitry 401. In the illustrated embodiment, color comparison circuitry 303 processes data on a pixel-by- pixel basis and is resynchronized with both the graphics back- end pipeline 205 and the video back-end pipeline 204 by having its outputs latched to the video clock (VCLK) by latches 404.

The output of color comparison circuitry 303 is passed to the "K" control input of overlay control multiplexer 304. The "P" control input to multiplexer 304 is provided from pixel position comparison circuitry 305. The data inputs to multiplexer 304 are coupled to an 8-bit overlay OP Code (OOC) register 306. The output of multiplexer 304 is used as one control input to output multiplexer 304, which along with a single bit set by CPU 101 into output control register 307, selects which of the data received at the data inputs of multiplexer 231 will be output to DAC 210.

Pixel position comparison circuitry 305 includes three inputs coupled respectively to video

window 1 position control circuitry 308, CRT position control circuitry 309 and video window 2 position control circuitry 310. In the illustrated embodiment, CRT position controller 309 is located within CRT controller 220 while video window 1 position control circuitry and video window 2 position control circuitry 310 are located within video display window controls 222 (FIG. 2). CRT position control circuitry 309 includes counters which, track the position of the current pixel being generated for display. In the preferred embodiment, CRT position control circuitry 309 includes at least an x-position counter which tracks the generation of each pixel along a given display line and a y-position counter which tracks the generation of each display line in a screen. The x-position counter may for example count pixels by counting each VCLK period between horizontal synchronization signal (HSYNC) controlling display unit 106. The y-position counter may for example count each HSYNC signal occurring between each vertical synchronization signal (VSYNC) controlling the screen generation on display unit 106. FIG. 4B is an alternate embodiment of the color comparison circuitry of FIG. 3. In a first mode, 8 bits are from attribute controller 233 are passed through multiplexer to comparator 406. Comparator 406 compares the received eight bits with an 8-bit color key in color key register 408; when the received 8-bits equal the 8-bit key 1, the output of comparator 406 goes active (high). In the first mode, control signal 16BITGR is high (and the output of NOR gate 409 is consequently high) and an active output from comparator 406 is gated through AND gate 410. The output of AND gate 410 is passed to AND gate 411 and gated with the output from the pixel comparison circuitry 305. The output of AND gate 411 goes directly to the "B" control input of selector 231 (in this embodiment multiplexer 304 and register 306 are eliminated). Thus, when the 8-bit graphics pixels output from attribute controller 233 of graphics backend 205 matches the 8-bit color key 1 and the window has been reached as determined by pixel comparison circuitry 305, the pixel data output from video backend 204 are passed through selector 231.

In a second mode, 16 bits are received from serializer 236. The eight LSBs are passed through multiplexer 405 to comparator 406 and the eight MSBs passed to comparator 407. Control signal 16BITNG is set high. When the LSBs equal key 1 in color register key 408 and the 8 MSBs equal key 2 in color key register 408, the outputs from comparators 406 and 407 are active (high). The output of AND gate 411 then goes high when the output from pixel comparison circuitry 305, which is coupled to the "B" control input of selector 231, goes high. Thus, when the 16-bit pixel data output from serializer 236 of graphics backend 205 matches the 16- bit color key (keys 1 and 2) and a window has been reached, the output pixel data from video backend 204 are passed through selector 231.

FIG. 5 is an expanded functional block diagram of the video window position control circuits 308 and a corresponding portion of the gating of pixel position compare circuitry 305. Each position control circuit 310/312 is coupled to a screen position x-register 500 and a screen position y- register 501, and includes a screen x-position counter 502, and a screen y- position counter 503. In the preferred embodiment, registers 500 and 501 are located within video window control registers 203. For the window corresponding to the given video window control circuitry 308 or 310, registers 500 and 501 are loaded with a value representing the x and y screen position of the pixel in the upper left corner of that window (the starting pixel). Screen x- register 500 and screen y-register 501 in the preferred embodiment are loaded by CPU 101. The screen x-position counter 502 counts down from the value held in screen x-register 500 with each video clock when P is high for each display line and resets with each display horizontal synchronization signal (HSYNC) (Note that when P is high the CRT count matches the position count). Screen y-position counter 503 counts down from the value set into screen y- register 501 for each horizontal sync signal (HSYNC) at the start of each display line and resets with each VSYNC at the start of each new screen (The position counters are allowed to count only when they match their perspective CRT). The counts values in the counters of CRT position control circuitry 309 are compared pixel by pixel with the counts in screen x-position counter 502 and screen y- position 503 of each video window position control circuitry 308 and 310. When both the x and y counts in the counters of CRT position control circuitry 309 match the corresponding x and y counts in respective counters 502 and 503 of either video window control circuitry 308 or 310, the control signal P to

multiplexer 304 is activated. The activation of control signal P indicates that the raster scan on display 106 has reached the position of a pixel within the window and data from video pipeline 205 may be painted depending on the value being held in overlay OP Code (OOC) register 306 and the K control inputs to multiplexer 304.

A 4-bit OP Code loaded by CPU 101 into overlay OP Code register 306 in conjunction with the control signals applied to the "P" and "K" control inputs to multiplexer 304 control the presentation of an active (assumed high in the illustrated embodiment) control signal to the "B" control input to output multiplexer 231. The other ("A") input to output multiplexer 231 receives a bit from overlay mode register 402 (FIG. 4), as loaded by CPU 101. In the illustrated embodiment, the selection between the streams from the graphics and video backends at the 0,1,2 inputs to output multiplexer 304 in response to the signals presented at the corresponding control inputs "A" and "B" is in accordance with Table II:

Control Input A

Control Input B

Selected Stream

---

0 0 Graphics or

video pixels

from graphics

pipeline 205

1 0 Graphics pixels

from CLUT 234 at

input 1

0 1 Video or

1 1 graphics from

video backend

204

The OP Codes used in the illustrated embodiment, the effective overlay and the corresponding inputs to the control inputs of multiplexer 304 are listed in Table III (active state is assumed:

Overlay Op Code

Multiplexer 307

Register 309 Value

Control Inputs

Effect

---

0 N/A Pixels passed

only from

graphics pipeline

205

A Input P active

Paint pixels from

video backend

pipeline 204 only

inside video

window VDW.sub.n

8 Inputs K and P

Paint from video

active backend pipeline

204 window VDW.sub.n

when color key

matches

C Inputs K active

Paint from video

backend pipeline

204 if color key

matches

In the illustrated embodiment, if a Oh is written into OOC register 306 by CPU 101, only pixels from graphics pipeline 205 are pipelined through multiplexer 304. In this case any signals applied to the P and K control inputs to multiplexer 304 have no effect (i.e., will not result in a high output from multiplexer 304). In the illustrated embodiment, if an Ah is written into OOC register 306, pixels from video pipeline 204 will be passed to DAC 210 only when pixel position comparison circuitry 305 determines that the raster scan has reached a pixel in the window and hence the control signal going to the P input of multiplexer 304 has been activated. If on the other hand, an 8h is written into OOC register 306, data is passed through output multiplexer 231 to DAC 210 when pixel

position comparison circuitry 305 determines that the raster scan has reached a pixel on the display screen within the window and color compare circuitry 302 has determined that the incoming data from graphics pipeline 205 matches the overlay color key held in overlay color key register 303. In this case, the data from video pipeline 204 is passed to DAC 210 when both the P and the K inputs to multiplexer 304 are active. Finally, when an OpCode of C is programmed into OOC register 306, data from video pipeline 204 is passed if the incoming data from graphics pipeline 205 matches the overlay color key held in overlay color key register 303. In this case, the activation of the K control input activate the output of multiplexer 304 to switch the input of multiplexer 231 to pass the corresponding video pixels.

Display control circuits embodying the principles of the present invention have substantial advantages over the prior art. In particular, output control circuits built in accordance with the principles of the present invention allow for the flexible display of both graphics and video on the same screen. In particular, pixel position comparison circuitry 305 along with video window position control circuits 308 and 310 and CRT position control circuitry 309 allow for a one or more windows from off-screen memory to be generated in specific areas of a display screen to the exclusion of any simultaneously generated data from on-screen memory. Further, color comparison circuitry 302 operating in conjunction with an overlay color key written into overlay color key register 303 allows window data to be presented on the display screen, to the exclusion of any concurrently generated graphics data, without the need for precise x- and y-position data for the window. Finally, the use of the graphics data from the graphics pipeline 205 to control the output overlay provides additional advantages since the video data can be subject to graininess and noise.

Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations an be made herein without departing from the spirit and scope of the invention as defined by the appended claims.

ENGLISH-CLAIMS:

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What is claimed is:

1. A graphics and video controller comprising:

an interface for receiving words of pixel data, each said word associated with an address buffer;

circuitry for writing each said word of said pixel data received by said interface to a one of on-screen and off-screen memory areas of a frame buffer;

circuitry for selectively retrieving said words from said on- screen and off-screen areas;

a first pipeline for processing words of graphics data retrieved from said frame buffer; and

a second pipeline for processing words of video data retrieved from said frame buffer.

2. The controller of claim 1 and further comprising output selection circuitry for selecting for output between graphics data received from said first pipeline and data received from said second pipeline, said selection circuitry operable to:

in a first mode, pass data from said first pipeline: and

in a second mode, pass data from said second pipeline when said data corresponds to a selected display position of a display window.

3. The controller of claim 2 wherein said selection circuitry is further operable to:

in a third mode, pass data from said second pipeline when said data corresponds to said selected display position of said display window and data from said first pipeline match a color key.

4. The controller of claim 3 wherein said selection circuitry is further operable in a fourth mode to pass data from said second pipeline when data from said first pipeline match a color key.

5. The controller of claim 1 wherein said circuitry for retrieving maintains a stream of graphics data to said first pipeline and provides video data to said second pipeline when a display raster scan reaches said display position of said window.

6. The controller of claim 1 and further comprising:

a video port for receiving real-time video data; and

circuitry for generating an address to said memory at which said real- time video data is to be stored.

7. The controller of claim 1 wherein said second pipeline includes a first first-in-first-out memory for receiving data for a first display line of pixels in memory and a second first-in-first-out memory for receiving data from a second display line of pixels memory.

8. The controller of claim 7 wherein said first display line adjacent in memory to said second display line.

9. The controller of claim 7 wherein said output selection circuitry comprises:

an output selector for selecting between data from said second pipeline and data from said first pipeline in response to a selection control signal;

a register for maintaining a plurality of overlay control bits;

window position control circuitry for selectively generating a position control signal when a word of said data stream from said second pipeline falls within a display window;

color comparison circuitry for comparing words of said data stream from said first pipeline with a color key and for providing in response a color comparison control signal; and

a control selector for selectively providing a said selection control signal in response to said overlay control bits in said register and at least one of said position control and color comparison control signals.

10. The controller of claim 9 wherein said window position control circuitry comprises:

window position counters operable to increment from initial count values corresponding to a starting pixel of a display window as data representing each pixel in a display screen is pipelined through said overlay control circuitry;

screen position counters operable to count as data representing each pixel in said display screen is pipelined through said overlay control circuitry; and

comparison circuitry operable to compare a current count in said window position counters and a current count in said screen position counters and selectively generate said position control signal in response.

11. The controller of claim 9 wherein said color comparison circuitry comprises:

a color key register for storing bits composing said color key; and

a plurality of AND-gates for comparing said words of said graphics data stream with bits of said color key.

12. The controller of claim 1 wherein said interface includes a dual- aperture port.

13. A controller comprising:

circuitry for writing selectively each word of received data into s selected one of on-screen and off-screen memory spaces of a frame buffer;

a first port for receiving video and graphics data, a word of said data received with an address of said memory spaces directing said word to be processed as a word of video data or a word of graphics data;

a second port for receiving real-time video data;

circuitry for generating an address associated with a selected one of said memory spaces for a word of said real-time video data;

circuitry for selectively retrieving said words of data from said on- screen and off-screen memory spaces as data is rastered for driving a display;

a graphics backend pipeline for processing ones of said words of data representing graphics data retrieved from said frame buffer;

a video backend pipeline for processing other ones of said words of data representing video data retrieved from said frame buffer, said circuitry for retrieving always rastering a stream of data from said frame buffer to said graphics backend pipeline and rastering video data to said video backend pipeline when a display raster scan reaches a display position of a window; and

output selector circuitry for selecting for output between words of data output from said graphics backend pipeline and words of data output from said video backend pipeline.

14. The controller of claim 13 wherein said output selector is further operable to select between graphics data output from a color look- up table and true color data output from said graphics pipeline.

15. The controller of claim 13 wherein said output selector is operable to:

in a first mode, pass only a word of data output from said graphics pipeline;

in a second mode, pass a word of data output from said video pipeline when said display raster scan has reached a display position corresponding to a window and a word of data from said graphics pipeline when said display raster scan is in any other display position;

in a third mode, pass a word of data output from said video pipeline when said display raster scan has reached a display position corresponding to a window and a corresponding word of data from said graphics pipeline matches a color key and a word of data from said graphics pipeline when said display raster scan is in any other display position; and

in a fourth mode, pass a word of data from said video pipeline when said corresponding word of data from said graphics pipeline matches a color key and a word of data from said graphics pipeline when said display raster scan is in any other display position.

16. The controller of claim 13 wherein said video pipeline includes a first first-in-first-out memory for receiving a plurality of words of data for a first display line of pixels in memory and a second first-in- first-out memory or receiving a plurality of words of data from a second display line of pixels in memory.

17. The controller of claim 16 wherein said first display line is stored adjacent in memory to said second display line.

18. The controller of claim 13 wherein said output selector circuitry comprises:

a control selector having a plurality of control inputs coupled to a register, said register storing a plurality of overlay control bits;

window position control circuitry coupled to a first control input of said control selector, said window position control circuitry operable to selectively provide a first control signal to said first control input when a word of data being pipelined through said video pipeline falls within a display window;

color comparison circuitry operable to compare a word of data being pipelined through said graphics pipeline with a color key and provide in response a second control signal to a second control input of said control selector; and

wherein said control selector is operable to provide an output selection control signal in response to at least one of said first and second control signals and said overlay control bits being stored in said register.

19. The circuitry of claim 18 wherein said output selector circuitry further includes a third control input coupled to certain bits of said graphics pipeline, said output selector further operable to select between data on said respective video and graphics pipelines in response to said certain bits presented to said selector circuitry.

20. The circuitry of claim 18 wherein said window position control circuitry comprises:

a window x-position counter operable to count from a loaded x- position value in response to a video clock, said x-position counter reloading in response to display horizontal synchronization signal;

a window y-position counter operable to count from a loaded y- position value in response to said horizontal synchronization signal, said y- position counter reloading in response to a display vertical synchronization signal;

CRT position circuitry operable maintain counts corresponding to a current display pixel; and

comparison circuitry operable to compare current counts in said window counters with said current counts held in said CRT position circuitry and generate in response said first control signal.

21. The circuitry of claim 20 wherein said window position control circuitry further comprises an x-position register for holding said x- position value for loading into said x-position counter and a y- position register for holding said y-position value for loading into said y- position counter.

22. The circuitry of claim 13 wherein said color comparison circuitry comprises:

a color key register for storing a plurality of color key bits; and

a plurality of XNOR-gates each having at least one input coupled to a bit position in said color key register and at least one input coupled to said graphics data path.

23. The circuitry of claim 13 wherein said video pipeline comprises:

a first-in/first-out memory for receiving a first stream of words of data from said frame buffer;

a second first-in/first-out memory disposed in parallel with said first first-in/first-out memory for receiving a second stream of words of data from said frame buffer; and

interpolation circuitry for selectively generating an additional word of data by interpolating a word of said first stream and a word of second stream data output from said first and second first- in/first-out memories.

24. The controller of claim 13 wherein said first pore comprises a dual-aperture port.

25. A display system comprising:

a first backend pipeline for processing data;

a second backend pipeline for processing graphics data disposed in parallel to said first processing pipeline;

a multi-format frame buffer memory having on-screen and off- screen areas each operable to simultaneously store data in graphics and video formats;

a input port for receiving both graphics and video data, each word of said data associated with an address directing said word to be processed as either graphics or video data;

circuitry for writing a word of said playback data into a selected one of said areas of said multi-format memory;

memory control circuitry for controlling the transfer of data between said first backend pipeline and said frame buffer and between said second backend pipeline and said frame buffer;

a display unit; and

overlay control circuitry for selecting for output to said display unit between data provided by said first backend pipeline and data provided by said second backend pipeline.

26. The display system of claim 25 wherein said second backend pipeline includes:

a first first-in-first-out memory for receiving first selected data;

a second first-in-first-out memory disposed in parallel to said first first-in-first-out memory for receiving second selected data;

interpolation data for generating additional data by interpolating data output from said respective first and second first-in- first-out memories.

27. The display system of claim 26 wherein said second backend pipeline further comprises color conversion circuitry for converting data received from said frame buffer in a video format to a graphics format.

28. The display system of claim 25 and further comprising a video front-end pipeline for inputting video data into a selected one of on- screen and off-screen spaces of said frame buffer comprising:

a video data port for receiving video data from a real time data source;

input control circuitry for receiving framing signals associated with said real time data and generating corresponding addresses to said selected one of said spaces in response.

29. The display system of claim 28 wherein said video front- end pipeline further comprises encoding circuitry for packing said video data prior to storage in said selected

one spaces.

30. The display system of claim 28 wherein said video front- end pipeline further comprising multiplexing circuitry for selecting between video data received through said video data port and data received from said dual aperture port.

31. The display system of claim 30 wherein said video front end pipeline further comprises conversion circuitry for converting graphics data received through said dual-aperture port to a video format for storage in said selected one of said spaces.

32. The display system of claim 25 wherein said first backend pipeline processes playback video.

33. The display system of claim 25 wherein said input port comprises a dual-aperture input port.

34. A display data processing system comprising:

circuitry for writing data into an on-screen space of a frame buffer;

circuitry for writing data into an off-screen space of said frame buffer;

a video pipeline for processing data output from a selected one of said on-screen and off-screen spaces comprising:

a first first-in-first-out memory for receiving selected data from said selected space;

a second first-in-first-out memory disposed in parallel to said first first-in-first-out memory for receiving other selected data from said selected space; and

an interpolator for generating additional data by interpolating data output from said respective first and second first-in- first-out memories;

a graphics pipeline disposed in parallel to said video pipeline for processing data output from a selected one of said on-screen and off- screen spaces; and

an output selector for selecting between data output from said video pipeline and data output from said graphics pipeline.

35. The system of claim 34 and further comprising selection control circuitry for generating an output control signal for controlling said output selector comprising:

a control selector having a plurality of data inputs coupled to a register, said register for storing a plurality of overlay control bits; and

color comparison circuitry operable to compare bits of data output from said graphics pipeline with a color key and provide in response a control signal to a control input of said control selector.

36. The system of claim 34 and further comprising window position control circuitry operable to provide a second control signal to a second control input of said control selector when data from said video pipeline falls within a display window.

37. A display controller comprising:

circuitry for selectively retrieving data from an associated multi- format frame buffer for simultaneously snoring graphics and video data;

a first pipeline for processing words of graphics data selectively retrieved from said frame buffer; and

a second pipeline for processing words of video data selectively retrieved from said frame buffer.

38. The controller of claim 37 wherein said first and second pipelines are disposed in parallel and concurrently process data.

39. The controller of claim 38 and further comprising output selection circuitry for selecting for output between graphics data received from said first pipeline and video data received from said second pipeline.

40. The controller of claim 37 wherein said frame buffer is partitioned into on-screen and off-screen areas, each of said on-screen and off-screen areas operable to simultaneously store both graphics and video data.

41. The controller of claim 37 wherein said circuitry for selectively retrieving is operable to retrieve a constant stream of graphics data from said frame buffer and provide said stream of graphics data to said first pipeline.

42. The controller of claim 41 wherein said circuitry for selectively retrieving is operable to retrieve at least one said word of video data from said frame buffer and provide said at least one word of said video data to said second pipeline, only when said display controller is generating a video display window.

43. A display controller for interfacing a multi-format frame buffer and a display device, the multi-format frame buffer having on- screen and off- screen areas each for simultaneously storing both graphics and video pixel data, said display controller comprising:

circuitry for selectively retrieving pixel data from a selected one of said on-screen and off-screen areas of said frame buffer;

a graphics backend pipeline for processing graphics data retrieved from said selected one of said areas of said frame buffer;

a video backend pipeline for processing video data retrieved from said selected one of said areas of said frame buffer; and

an output selector for selectively passing to said display device data received from said graphics or video backend pipelines.

44. The display controller of claim 43 wherein said circuitry for selectively retrieving is operable to retrieve at least one said word of video data from said frame buffer and provide said at least one said word of video data no said second pipeline only when said display controller is generating a video display window.

45. The display controller of claim 43 wherein said output selector is operable to:

in a first modes pass data from said graphics pipeline; and

in a second modes pass data from said video pipeline when a display position corresponding to a video display window has been reached.

46. The display window of claim 43 wherein said output selector is operable to:

in a first mode, pass data from said graphics pipeline; and

in a second mode, pass data from said video pipeline when a display position corresponding to a video display window has been reached and data from said graphics pipeline match a color key.

47. The display controller of claim 43 wherein said output selector is operable to:

in a first mode, pass data from said graphics pipeline; and

in a second mode, pass data from said video pipeline when data from said graphics pipeline matches a color key.

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*1999 ITC LEXIS 225, **

In the Matter of CERTAIN VIDEO GRAPHICS DISPLAY CONTROLLERS AND PRODUCTS CONTAINING SAME

Inv. No. 337-TA-412

1999 ITC LEXIS 225

UNITED STATES INTERNATIONAL TRADE COMMISSION

July 19, 1999

CORE TERMS: patent, domestic industry, notice, initial determination, invalidity, infringement, importation, infringe, graphics, selling, video, final determination, administrative law, contingent, telephone, invalid

DETERMINATION:

[*1]

NOTICE OF COMMISSION DETERMINATION NOT TO REVIEW THE BULK OF AN INITIAL DETERMINATION FINDING NO VIOLATION OF SECTION 337 OF THE TARIFF ACT OF 1930

INFORMATION:

SUMMARY: Notice is hereby given that the U.S. International Trade Commission has determined not to review, as explained below, the presiding administrative law judge's final initial determination (ID) and has thereby made a final determination of no violation of section 337 of the Tariff Act of 1930, as amended, in the above-captioned investigation.

FOR FURTHER INFORMATION CONTACT: Clara Kuehn, Esq., Office of the General Counsel, U.S. International Trade Commission, 500 E Street, S.W., Washington, D.C. 20436, telephone (202) 205-3012. Hearing-impaired persons are advised that information on this matter can be obtained by contacting the Commission's TDD terminal on 202-205-1810. General information concerning the Commission may also be obtained by accessing its Internet server (*http://www.usitc.gov*).

SUPPLEMENTARY INFORMATION:

The Commission ordered the institution of this investigation on July 27, 1998, based on a complaint filed on behalf of Cirrus Logic, Inc., Fremont, California ("Cirrus" or "complainant"). 63 *Fed. Reg.* 40932 (1998). **[*2]** The notice of investigation was published in the *Federal Register* on July 31, 1998. *Id.* The complaint alleged that ATI Technologies, Inc., Thornhill, Ontario, Canada ("ATI" or "respondent") violated section 337 of the Tariff Act of 1930, as amended, 19 U.S.C. § 1337, by importing, selling for importation, and selling in the United States after importation certain video graphics display controllers that infringe claims 37 and 43 of Cirrus' U.S. Letters Patent **5,598,525** ("the '525 patent"). *Id.* On October 29, 1998, the presiding administrative law judge (ALJ) issued an ID (ALJ Order No. 14) granting Cirrus' motion to amend the complaint and notice of investigation to add allegations of infringement of claims 1-10, 12-21, and 23-24 of the '525 patent, and that ID was not reviewed by the Commission. 63 *Fed. Reg.* 66581 (1998).

The ALJ held a tutorial on the technology for displaying video and graphics data on personal computers on January 7, 1999. On January 20, 1999, Cirrus filed a notice of withdrawal of certain disputed claims, indicating that only claims 13, 15, 16, 17, 23, and 37 remained in dispute. An **[*3]** evidentiary hearing was held from January 21, 1999, to January 29, 1999.

The ALJ issued her final ID on April 30, 1999, concluding that there was no violation of section 337, based on the following findings: (a) complainant failed to establish the requisite domestic industry; (b) the asserted claims of the '525 patent, claims 13, 15, 16, 17, 23, and 37, are invalid; and (c) assuming, *arguendo*, the validity of the asserted claims, respondent's accused devices do not infringe the asserted claims. On May 11, 1999, the ALJ issued her recommended determination on remedy and bonding, in the event the Commission were to conclude there is a violation of section 337.

On May 13, 1999, complainant filed a petition for review of the ID, arguing that the ALJ erred in construing specific terms in claims 13, 15, 16, 17, and 23, erred in her invalidity and infringement analyses of those claims, and erred in concluding that complainant did not satisfy the domestic industry requirement. Complainant's petition included a request for contingent review of the ALJ's conclusions concerning certain prior art and her construction of additional terms in these claims, should the Commission adopt complainant's **[*4]** claim construction over the ALJ's. Complainant did not petition for review of the ALJ's conclusions as to claim 37. Respondent filed a contingent petition for review identifying as issues for consideration should the Commission decide to review the ID certain aspects of the ALJ's construction of claims 13, 15, 16, 17, 23, and 37, application of the doctrine of equivalents, and conclusions as to invalidity and inequitable conduct. The Commission investigative attorney (IA) petitioned for review of the ALJ's alternative basis for finding no domestic industry as erroneous as a matter of law. On May 20, 1999, respondent, complainant, and the IA filed responses to the petitions for review.

Having reviewed the record in this investigation, including the parties' written submissions, the Commission determined not to review the ID, except that the Commission determined to take no position as to the ALJ's findings as to the following issues: (1) the invention date of the '525 patent; (2) the prior art status of the Oak/Brooktree combination under 35 U.S.C. § 102(a); (3) the prior art status of the Bindlish '864 patent under 35 U.S.C. § 102 **[*5]** (e); (4) the invalidity of claim 37 of the '525 patent as anticipated by the Bindlish '864 prior art patent under 35 U.S.C. § 102(e); and (5) the non-enablement of claims 13, 15, 16, 17, and 23. With respect to the ID's finding that complainant failed to satisfy the technical prong of the domestic industry requirement in part because claim 13 is invalid for indefiniteness, the Commission clarifies that it understands the ID to mean that complainant cannot meet the burden of demonstrating the practice of an indefinite claim. The Commission thereby adopted the ID, with the exceptions noted, as its final determination.

The authority for the Commission's determinations is contained in section 337 of the Tariff Act of 1930, as amended (19 U.S.C. § 1337), and in sections 210.42-210.43 of the Commission's Rules of Practice and Procedure (19 C.F.R. §§ 210.42-.43).

Copies of the public version of the ALJ's ID and all other nonconfidential documents filed in connection with this investigation are or will be available for inspection during official business hours (8:45 a.m. to 5:15 p.m.) in the Office of the Secretary, U.S. **[*6]** International Trade Commission, 500 E Street, S.W., Washington, D.C. 20436, telephone 202-205-2000.

CERTIFICATE OF SERVICE

I, Donna R. Koehnke hereby certify that the attached **NOTICE OF COMMISSION DETERMINATION NOT TO REVIEW THE BULK OF AN INITIAL DETERMINATION FINDING NO VIOLATION OF SECTION 337 OF THE TARIFF ACT OF 1930**, was served upon the following parties via first class mail and air mail, where necessary, on **July 19, 1999.**

Donna R. Koehnke, Secretary

U.S. International Trade Commission

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Washington, D.C. 20436

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